CLOCKLESS CHIPS

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Abstract

Several undesirable features of synchronous chips have emerged with the increase in the frequency of the clock used to operate them. Clockless chips dispense with the clock entirely to overcome these drawbacks of synchronous chips. Clockless chips use asynchronous techniques to achieve synchronisation between its various components. They run much faster, consume much less power and are much smaller in size than their synchronous counterparts. It has been anticipated that the clockless technology will drive most of the electronics chips in the foreseeable future.

Keywords: Clockless chips, Bounded delay method, Delay insensitive method, NULL convention logic, Asynchronous design

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1. Introduction

The speed of a digital computer is generally specified in terms of the frequency of a tiny clock inside it, namely a crystal oscillator that generates clock signals at a specific rate. For example, a crystal with a frequency of 1 GHz generates $10^9$ clock signals per second. These clock signals synchronise all the activities inside the machine.

Every action of the computer takes place in a sequence of small steps. A simple data transfer may take only one step, whereas a complex calculation may take hundreds of steps. However, all steps must begin and end according to the clock signals that the crystal oscillator generates.

Due to the desire for greater computational speed, the clock frequency has been rapidly increasing. Distributing the high frequency clock signal throughout the entire chip has become more complicated. Clock frequencies are now in the gigahertz range, and are close to the physical limits. The signals barely have enough time to move across the chip before the next clock signal begins. Increasing the clock frequency beyond the physical limits could have disastrous consequences.

Present day transistors can complete several steps in the time that it takes a signal to go from one side of the chip to another. Maintaining synchronism throughout a large chip requires careful design and considerable electrical power. In this scenario, therefore, a need has arisen for an alternative to the clocked chip design.

The proposed alternative suggests dispensing with the clock entirely. This approach, known as the clockless chip, uses a technique known as asynchronous logic. It differs from a conventional computer circuit in that the switching of the digital circuits is controlled individually by specific pieces of data, rather than by a universal clock that forces all the circuits on the chip to operate in unison. It overcomes all the disadvantages of a clocked circuit such as slow speed, high power consumption, and high electromagnetic noise.

The clockless technology is considered as the technology that will drive majority of the electronics chips in the foreseeable future.
2. Synchronous Circuits

The clock is a tiny crystal oscillator that resides in the heart of every microprocessor chip. It synchronises the motion of electrons throughout the millions of wires and transistors of a digital computer. Such crystals, which generate frequencies of about 4 GHz in the fastest of today’s desktop personal computers, dictate the timing of operation of every circuit in every chip, that perform a wide range of functions ranging from moving binary data to performing complex mathematical calculations. These conventional synchronous chips, which operate under the control of a central clock, process the data in the registers at precise time intervals.

Figure 1 Synchronous circuit

Figure 1 shows the working model of a synchronous circuit. In this example, the circuit performs all actions on the leading edge of the clock pulse. When transferring data between registers, the circuit waits for the next leading edge to occur. The data will be transferred only when the leading edge occurs. Designers of the synchronous chips have only to ensure that the circuit completes one operation within one clock cycle, and that all computations are complete and the data is ready for the next operation before the beginning of the next clock cycle.
3. Clockless Chips

A clockless chip, as the name suggests, does not have a global clock to synchronise its actions. These chips rely on handshaking signals, and sometimes a local clock to synchronise its actions.

Clockless chips draw power only when there is useful work to do, resulting in huge power conservation in battery driven devices. Like a team of horses that can only run as fast as its slowest member, a clocked chip can run only as fast as its slowest piece of logic, since the answer is not guaranteed until every component has completed its work. By contrast, the transistors on a clockless chip can transfer information independently, without the need to wait for everything else. As a result, the entire chip can run at the average speed of all components.

![Clockless Circuit Diagram](image)

Figure 2 Clockless circuit

Figure 2 shows the working of a clockless circuit. In this particular scheme (known as the dual rail circuit, which will be discussed later), data moves under the control of local handshake signals that indicate when the data is ready for the next operation. The two lines seen in Figure 2 are used together to transfer the both the data bits and the control bits. The control signal is encoded within the data being transferred.
4. Implementation of Clockless Chips

**General Model of a Clockless Circuit**

![General model of a clockless circuit](image)

*Figure 3* General model of a clockless circuit

Figure 3 shows the general model of a clockless circuit. The logic circuit performs the same operation as in the synchronous circuit. The completion detection circuit attached to it indicates when the logic circuit has completed its operation. The input signal and the “go” signal reach the unit simultaneously. When the logic circuit completes its operation, the completion detection circuit produces a “done” signal, which is an indication that the signal is ready to pass to the next step. In some cases the “done” signal acts as the “go” signal to the next stage.

There are mainly three kinds of implementations of an asynchronous circuit, namely:

1. Bounded Delay Method
2. Delay Insensitive Method
3. NULL Convention Logic (NCL)

**Bounded Delay Method**

![Bounded delay method model](image)

*Figure 4* Bounded delay method model
Figure 4 shows the bounded delay method model. This method is similar to the design of synchronous circuits. In this method, we assume that we know the maximum time a component takes to complete its operation. We transfer control to the next circuit only after this maximum time, known as the prototype delay, has elapsed.

The circuit which introduces this prototype delay acts as the completion detection circuit. In this method, a component is assumed to have completed its working when the introduced prototype delay is over.

The disadvantage of this method is that it is not possible to give the “done” signal as soon as the component completes its operation. The circuit has to wait until the prototype delay time is over, even if it completes its operation early.

*Delay Insensitive Method*

The delay insensitive method does not assume any time limits, and uses handshaking signals to synchronise the operations of different components. It can be implemented in several ways. The most common method is the “dual rail encoding” method. This method uses two channels to communicate the data and the control signals between various components. The signals on both the channels together indicate the data and the control signals. In one such method, a signal X is encoded with two wires XH & XL. The encoding scheme is as shown in Table 1.

<table>
<thead>
<tr>
<th>XH</th>
<th>XL</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Data not ready</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Logic 0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Logic 1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Don’t care</td>
</tr>
</tbody>
</table>

*Table 1* Dual rail encoding
As seen in Table 1, two signals are needed to implement the dual rail equivalent of each conventional circuit signal. Hence, special gates are required to implement the digital logic using dual rail encoding. The AND, OR, and NOT gates are shown in Figure 5.

![Figure 5](image)

**Figure 5** (A) AND gate (B) OR gate (C) NOT gate

**NULL Convention Logic**

NULL Convention Logic (NCL) integrates data transformation and control into a single expression, thus yielding inherently clockless systems. It enables digital designs for critical power, noise, or system integration issues.

NCL uses two states, namely a NULL state when the data is not ready, and a DATA state when the data is ready. The output of an NCL gate is NULL if it has any NULL input. Its output is DATA when all its inputs are DATA. Hence, the NCL gates do not need any clock since they perform their operation as soon as they receive their inputs.
NCL circuits switch between voltage based representation of DATA and a control representation of NULL. This separation provides a self synchronization throughout the entire digital circuit.

The basic building block of an NCL circuit is a threshold gate with hysteresis. Threshold gate inputs and outputs can be in one of the two states, DATA and NULL. A threshold gate output in NULL state will remain in NULL state until all its inputs are in the DATA state. It remains in the DATA state until all its inputs are brought into the NULL state.

The hysteresis in the threshold gate prevents switching of the output state to DATA, when number of inputs in DATA state increases, but is less than the threshold limit. It also enables to retain the output in DATA state until all inputs have returned to NULL.

![Figure 6 Block diagram of NCL](image)

Figure 6 shows the block diagram of the NCL. When the right register state is NULL, the completion detection block sends a request for DATA to the left register. The combinational circuitry evaluates the logic when all the inputs are available. The right register state switches to DATA and the result is passed to the next stage. The completion detection block sends the left register a request for NULL to reset the right register into the NULL state.
5. Benefits and Limitations of Clockless Chips

Primary Benefits

Clockless chips provide several benefits over the clocked chips. The primary benefits are discussed below.

1. Higher speed

A clocked chip can run only as fast as its slowest logic component, since the result is not guaranteed until every part completes its operation. Hence, if one component of the chip is much slower compared to the others, all other components are forced to sit idle, resulting in wastage of computing time.

By contrast, the transistors on a clockless chip can transmit and receive information independently, without the need to wait for everything else. As a result, the entire chip can run at the average speed of all components, rather than the speed of its slowest component. Therefore the speed of a clockless design is not limited by the size of the chip. Both Intel and Sun have developed clockless prototype chips that run two to three times faster than similar clocked products. The clockless Pentium designed by Intel in 1997 runs three times as fast as the synchronous equivalent.

2. Lesser power consumption

A clockless chip consumes less power than a clocked chip. The clock not only consumes more power than any other component on the chip but also occupies considerable area on the chip. The most undesirable aspect is that the clock serves no direct computational use. Further, as long as the chip is running, the clock consumes power continuously, while clockless chips consume power only during computations, and the idle parts of a clockless chip consume negligible amount of power.

The transistor density on a chip is continuously increasing. As the number of transistors on a chip increases, so does the power consumed by the clock. An increasing number of chips are being developed for use in mobile devices, which are essentially battery operated. Power conservation and smaller device size are crucial for such devices. Hence, clockless chips are highly appropriate for mobile applications.
Clockless Chips

The lower power consumption of the clockless chips can reduce the cost of design of equipments that are plugged to the power supply, such as personal computers, by reducing the need for cooling fans, air conditioners and other cooling equipments used to prevent overheating.

3. Lesser electromagnetic noise

A clockless chip produces much less electromagnetic interference than a clocked chip. A clocked chip emits strong signals at its operating frequency and at the harmonics of that frequency, which might interfere with other devices operating at similar frequencies. Clockless chips do not operate at a particular frequency so they radiate their energy over a broad frequency spectrum, thus emitting less energy at a particular frequency.

Nowadays, the demand for mobile devices is rapidly increasing. The operating frequency range of these devices is in gigahertz, which is similar to that of the present day clocks. The use of clocked chips in such devices limits the scale of integration since we need to avoid the electromagnetic interference caused by the clock at the operating frequency of the mobile device.

Other Benefits

Moving data between two computers controlled by different clock frequencies results in errors, because their operations are not synchronised. A clockless design can be used to build an asynchronous bridge between these two computers, which enables errorless data transfer.

Since the components of a clockless system need not operate at a common frequency, the designers have more flexibility in designing the components of a clockless system and in determining how these components interact. Moreover, replacing any component of a clockless system with a faster version will improve the speed of the entire system, whereas the increasing the speed of a clocked system usually requires upgrading every component.

Clockless chips also provide superior encryption because unlike clocked chips, it does not produce any regularly timed signals that an adversary may track.
Limitations

The design of clockless chips faces several limitations. Some of them have been discussed below.

1. Design difficulties

The primary drawback of clockless design is that it is difficult. The control logic must operate in the fundamental mode or burst mode, and the synthesis conventions are unfamiliar. Researchers have yet to make clockless design an algorithmic process.

Asynchronous design is not typically taught in the universities. Therefore, a company that decides to develop clockless chips must begin by training their engineers in the basics.

2. Lack of good tools

Another problem for clockless design is the predominant focus of CAD tools towards synchronous design. However, most circuit simulation tools are independent of synchrony, and may be easily adapted for asynchronous design.

3. Testing difficulties

Testing clockless circuits also presents several challenges. For example, in synchronous circuit testing, a common technique is to slow the clock to allow the logic computations to be observed at human speeds. Providing similar techniques for clockless circuit testing is quite complicated.

Timing requirements of a clockless circuit are more constrained than those of synchronous circuits. Whereas the latter have to simply provide a valid result before the next clock signal, clockless circuits may have minimum delays, such as the prototype delay in a bounded delay design.

Another difficulty in clockless circuit testing could be the necessity to test interleaving states during the computations.

Clockless control circuitry must handle a variety of timing events, and hence, the testing utility must be able to produce most of these events.
6. **Applications**

Clockless design is inevitable in the future of chip design because of two major advantages of speed and power consumption. However, before we begin to use them significantly in applications, several prototypes need to be developed and tested for reliability. Manufacturing techniques also need to be improved to make mass production of clockless chips feasible.

Clockless chips are expected to play a major role in mobile applications in the near future, due to minimal power consumption, reduced electromagnetic interference, and smaller chip size.

It may take some time before clockless designs are used in personal computers (PC) because of the competitive PC market. The manufacturing process should be improved to create an efficient design at a reasonable price.

Clockless chips may also be used for encryption since they do not give any regularly timed signals, and hence provide greater security against attacks. This might become all the more important as computers all over the world become more closely connected and share confidential material. Their excellent security also makes them suitable for use in smart cards.
7. Conclusion

The desire for faster computation by the synchronous chips has led to a rapid increase in their operating clock frequency. The clock frequencies have approached close to the physical limits of the synchronous chips, making their design more complicated. With the rise in demand for mobile devices, synchronous chips have also become undesirable due to the high power consumption and the high electromagnetic interference of the clock and its associated circuits.

Clockless chips, which use asynchronous logic, propose to solve this problem by removing the clock. Clockless chips operate without a central clock controlling the actions of all its components. These components achieve synchronisation by using asynchronous means, such as handshaking signals. Implementing clockless design requires special circuits that are differ from those used for conventional synchronous design.

A clockless chip operates much faster than a clocked chip because its components can perform their operations as soon as possible without waiting for a clock signal. It draws power only when required for the computation and hence, consumes considerably less power than a clocked chip. Since it does not operate at a particular frequency, it produces considerably less electromagnetic interference as compared to clocked chips. It is also smaller than a clocked chip due to the absence of the clock and the timing circuitry.

It may take a few years for clockless chips to be used on a large scale, due to the difficulties in the design, lack of good tools for design, and the difficulties in testing the designs. The scarcity of engineers with the required level of expertise to design clockless chips is also a hindrance that needs to be overcome. Finally, manufacturing processes need to be developed that make it feasible to mass produce reasonably priced and efficient clockless chips.

Owing to their several advantages over clocked chips and due to the rapid rise in demand for mobile devices, clockless technology is considered as the technology that will drive majority of the electronics chips in the foreseeable future.
## Appendix

<table>
<thead>
<tr>
<th>Company</th>
<th>Achievements</th>
<th>Goals</th>
</tr>
</thead>
<tbody>
<tr>
<td>SUN MICROSYSTEMS Palo Alto, CA</td>
<td>Prototypes have demonstrated two to three times the speed of standard chips.</td>
<td>Gradually integrate “islands” of clockless logic into future generations of microprocessors.</td>
</tr>
<tr>
<td>INTEL Santa Clara, CA</td>
<td>Clockless prototype in 1997 ran three times faster than the conventional chip equivalent, on half the power.</td>
<td>Stay current with clockless R&amp;D.</td>
</tr>
<tr>
<td>ASYNCHRONOUS DIGITAL DESIGN Pasadena, CA</td>
<td>Founded by students of Caltech’s Alain Martin, who developed the first asynchronous microprocessor</td>
<td>Produce chips for cell phones and other low power communications devices</td>
</tr>
<tr>
<td>THESEUS LOGIC Maitland, FL</td>
<td>Patented “null convention logic,” a way of letting clockless chips know when an operation is complete.</td>
<td>License designs to manufacturers of smart cards and mobile devices; Motorola is a current customer.</td>
</tr>
<tr>
<td>PHILIPS ELECTRONICS Eindhoven, Netherlands</td>
<td>Markets a clockless chip that gives its pagers up to twice the battery life of competitors</td>
<td>Clockless chips for mobile devices and smart cards.</td>
</tr>
<tr>
<td>SELF-TIMED SOLUTIONS Manchester, England</td>
<td>Founded Steve Furber who has developed clockless chips for communications devices</td>
<td>Clockless chips for smart cards.</td>
</tr>
</tbody>
</table>

Table 2 Clockless companies, their achievements and goals
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