THE INTEL MMX™ TECHNOLOGY

The Intel MMX™ technology comprises a set of instructions to the Intel architecture (IA) that are designed to greatly enhance the performance of advanced media and communications applications. These extensions (which include new registers, data types and instructions) are combined with the Single Instruction, Multiple Data (SIMD) Execution model to accelerate the performance of applications such as motion video, combined graphics with video, image processing, audio synthesis, speech synthesis and compression, 2D and 3D graphics, which typically use compute-intensive algorithms to accomplish the purpose. All existing soft wares that don't make use of this technology will also run on the processor without modification. Presented below is an elementary treatise on this technology in a programmer's point of view.

Overview of the MMX™ Technology Programming Environment

MMX™ technology provides the following new extensions to the Intel Architecture (IA) programming environment.

- Eight MMX™ registers (MM0 to MM7).
- Four MMX™ data types
- The MMX ™ instruction set

MMX™ Registers

The MMX™ register set consists of eight 64-bit registers (Fig 1). The MMX™ instructions access the MMX™ registers directly using the register names MM0 through MM7. These registers can only be used to perform calculations on the MMX™ data types; they can never be used to address memory. Addressing of MMX™ instruction operands in memory are handled by using the standard IA addressing modes (immediate, register mode etc.) and the general purpose registers.

MM0
MM1
MM2
MM3
MM4
MM5
MM6
MM7

Figure 1. The MMX™ Register Set

The MMX ™ Data Types

The MMX™ technology defines the following new 64-bit data types

1. Packed Bytes — Eight bytes packed into one 64-bit quantity
2. Packed Words — Four 16-bit words packed into a 64-bit quantity
3. Packed Double Words — Two double words packed into a 64-bit quantity
4. Quad Word — One 64-bit quantity

The bytes in the Packed Bytes data type are numbered from 0 to 7 and the lower order bits of a 64-bit data are placed in the byte 0 whereas the higher order bits in the byte 7. Similarly Packed Word data type contains 4 words numbered from 0 to 4 and the lower order 16 bits are placed in the 0th word. Similar is the case with the other two data types. The MMX™ instructions move the packed data types (packed bytes, packed words or packed double words) and the quad word data types to and from the memory or from the IA general purpose registers in 64-bit blocks. However when performing arithmetic or logical operations on the packed data types, The MMX™ instructions operate in parallel on the individual bytes, as described by the Single Instruction Multiple Data Execution model

The Single Instruction Multiple Data (SIMD)

The SIMD instruction model can access up to 8 bytes at a time for arithmetic or logical operations using a single instruction at a time. Thus the SIMD Technique speeds up the software performance by allowing the same operation to be carried out on multiple data items in parallel. The MMX™ technology supports parallel operations on byte, word, and double word data elements when stored in MMX™ registers.

The SIMD execution model supported in the MMX™ technology directly addresses the needs of modern media, communications and graphics applications which often use sophisticated algorithms that perform the same operations on a large number of small data types. For example audio data is represented in the form of 16-bit (word) quantities. The MMX™ instructions can operate on 4 of these words simultaneously with one instruction. Video and graphics information are represented as 8-bit quantities. Here one MMX™ instruction can operate on 8 of these bytes simultaneously. The memory can also be accessed in the 32-bit mode.

The MMX™ Instruction Set

The MMX™ instruction set contains 57 instructions, which can be grouped in to the following categories. Automatically the data is treated as packed or quad by the type of instruction.

- Data transfer instructions - Transfer data b/w memory and MMX™ registers
- Arithmetic instructions - Perform the basic arithmetic operations
- Comparison Instructions - Logical comparison of the data
- Conversion Instructions - To convert one data type into another
- Logical Instructions - Performs bit wise AND, OR etc
- Shift Instructions - To make Arithmetic Shift
- Empty MMX™ State Instructions (EMMS) - To end an MMX™ routine session

Saturation Arithmetic and Wraparound Mode

The MMX™ technology supports new arithmetic capabilities known as Saturating arithmetic and the Wraparound mode. In saturation mode, the result of an operation which results in a value that exceeds that of a particular data type are 'saturated' to the maximum value of that data type. In the Wraparound mode, results of an operation, which results in an overflow or underflow, are truncated and the least significant bits are returned; that is carry is neglected. These methods have profound applications in color calculations.

Instruction Operands

All MMX™ instructions except the EMMS instruction, reference on two operands: the source and the destination operands. The source operand can reside in the memory or any of the MMX™ Register. But the destination lies at one of the MMX™ registers.

Guidelines for writing Applications using MMX™ Code

The CPUID instruction can be used to determine whether the processor supports the MMX™ instruction set. When the support for MMX™ technology is detected by the CPUID instruction, the 23rd bit (MMX™ Technology bit) in the feature flags to 1. That is two versions of the routines should be made: one with scalar instructions and the other with the MMX™ instructions; the application will call the appropriate routine according to the response of the CPUID instruction.

Courtesy: Intel Architecture, Intel Inc. Santa Clara, California