DEVELOPMENT OF GSM BASED EMBEDDED SYSTEM FOR PREPAID ENERGY METER.

Introduction: -

The concept of this project is similar as any mobile communication & this project is based on the embedded system. Embedded system means it is one that has computer hardware with the software embedded in the ROM.

According to industrial report, India ranks sixth in Global Electricity Consumption Index with 606 units of per – Capita, consumption every year. This is the estimate to be scaled up to 1000 unit by 2012.

Again studies have revealed that 36% of the power losses in the transmission & distribution.

Again there are two main problem of the MSEB are :-

1) Overdue
2) Theft of Electricity

The main concept of our project is to solve this two problem by using the GSM based prepaid energy meter.
EMBEDDED SYSTEM:

An embedded system is a combination of computing H/W & S/W, and perhaps additional mechanical or other parts, designed to perform a specific function. An embedded is a component with in some larger system.

By definition, all embedded system contents a processor and software but what other feature do they have in common? Certainly, in order to have software, there must be a placed to store the executable coed and temporary storage for run time data manipulation. This take the form of ROM and RAM, respectively; any embedded system will have the sum of the both.

If only a small amount of memory is required, it might be contained whit in the same chip as processor. Otherwise, one or both types of memory will reside in external memory chip.

Fig. (a) Shows the block diagram of GSM based prepaid energy meter using the embedded system.

![Communication Block Diagram](image)

**Communication Block Diagram**

Figure : Communication block diagram
This project deals with GSM based electricity prepaid billing system for domestic power billing & transmission. In this project Embedded based prepaid energy meter with the GSM module at customer side will read the consumption of energy & send the signal to the server for update and control the customer meter. Control the customer meter means sever after receiving signal it will update the particular meter and then check remaining balance & send the signal to the customer meter then customer meter will update. If server detects any meter balance unit zero then it disconnects the power supply by sending the signal to particular meter via GSM. When the user sends request for recharge his meter then the server search that particular meter ID for recharge the same meter. User can also interact with the control
unit using GSM meter for Balance enquiry. This project is divided into major parts that are briefly described in the following section.

1) The customer (meter) side.
2) GSM architecture.
3) Server side with GSM module.

**The Customer (meter) side :-**

![General block diagram of prepaid energy meter](image)

Fig.(c): General block diagram of prepaid energy meter

General block diagram of prepaid energy meter is shown in figure. From prepaid meter side, it sends its update after every particular time period. Server to update the same meter information can use this update data. It have the following blocks are described below.
CENTRALIZED ENERGY BILLING USING WIRELESS PRE-PAID ENERGY METER.

CONSUMER SIDE SCHEMATIC DIAGRAM

Fig.(d): circuit diagram of prepaid energy meter
**Voltage and current measurement:**

- In this voltage is considered as constant and current is measurement for consumption in terms of power as

\[ P = I^2R \text{ watt} \]

- This measured current or power is converted into pulses by ADC measured by counter in the Microcontroller8051 and temporary stored in EEPROM and memory for compare with balance.

**ADC:**

- In this project we have used ADC 804IC
- ADC convert analog signal i.e. power into digital number or pulses.
- These pulses are given to IC NE555

**IC NE555:**

**DESCRIPTION**

The 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA.
FEATURES:

- Turn-off time less than 2 μs
- Max. Operating frequency greater than 500kHz
- Timing from microseconds to hours
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C

PIN CONFIGURATIONS:

APPLICATIONS:

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
MICROCONTROLLER:

The 8051 is the original member of the **MCW-51** family, and is the core for all MCS-51 devices. The features of the 8051 core is -

- 8-bit CPU optimized for control applications
- Extensive Boolean processing (Single-bit logic) capabilities
- 64K Program Memory address space
- 64K Data Memory address space
- 4K bytes of on-chip Program Memory
- 128 bytes of on-chip Data RAM
- 32 bidirectional and individually addressable I/O lines
- Two 16-bit timer/counters
- Full duplex UART
- 6-source/5-vector interrupts structure with two priority levels
- On-chip clock oscillator
- The basic architectural structure of this 8051 core is shown in Figure:

SFR:

A Map of the on-chip memory area called the Special Function Register (SFR) space is shown in Figure. Note that in the SFRs not all of the addresses are occupied. Unoccupied addresses are not implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have no effect. User software should not write 1s to these unimplemented locations, since they may be used in other 80C51 Family derivative products to invoke new features. The functions of the SFRs are described in the text that follows.
Accumulator:

ACC is the Accumulator register. The mnemonics for Accumulator-Specific instructions, however, refer to the Accumulator simply as A.

B Register:

The B register is used during multiply and divide operations. For other instructions it can be treated as another scratch pad register.

Program Status Word:

The PSW register contains program status information as detailed in Figure.

Stack Pointer:

The Stack Pointer register is 8 bits wide. It is incremented before data is stored during PUSH and CALL executions. While the stack may reside anywhere in on-chip RAM, the Stack Pointer is initialized to 07H after a reset. This causes the stack to begin at locations 08H.
Data Pointer:

The Data Pointer (DPTR) consists of a high byte (DPH) and a low byte (DPL). Its intended function is to hold a 16-bit address. It may be manipulated as a 16-bit register or as two independent 8-bit registers.

Ports 0 to 3:

P0, P1, P2, and P3 are the SFR latches of Ports 0, 1, 2, and 3, respectively. Writing a one to a bit of a port SFR (P0, P1, P2, or P3) causes the corresponding port output pin to switch high. Writing a zero causes the port output pin to switch low. When used as an input, the external state of a port pin will be held in the port SFR (i.e., if the external state of a pin is low, the corresponding port SFR bit will contain a 0; if it is high, the bit will contain a 1).

Serial Data Buffer:

The Serial Buffer is actually two separate registers, a transmit buffer and a receive buffer. When data is moved to SBUF, it goes to the transmit buffer and is held for serial transmission. (Moving a byte to SBUF is what initiates the transmission.) When data is moved from SBUF, it comes from the receive buffer.

Timer Registers:

Register pairs (TH0, TL0), and (TH1, TL1) are the 16-bit Counting registers for Timer/Counters 0 and 1, respectively.

Control Register:

Special Function Registers IP, IE, TMOD, TCON, SCON, and PCON contain control and status bits for the interrupt system, the Timer/Counters, and the serial port. They are described in later sections.
Port Structures and Operation:

All four ports in the 80C51 are bidirectional. Each consists of a latch (Special Function Registers P0 through P3), an output driver, and an input buffer. The output drivers of Ports 0 and 2, and the input buffers of Port 0, are used in accesses to external memory. In this application, Port 0 outputs the low byte of the external memory address, time-multiplexed with the byte being written or read. Port 2 outputs the high byte of the external memory address when the address is 16 bits wide. Otherwise, the Port 2 pins continue to emit the P2 SFR content. All the Port 3 pins are multifunctional. They are not only port pins, but also serve the functions of various special features as listed below:

**Port**

**Pin Alternate Function**

P3.0 RxD (serial input port)

P3.1 TxD (serial output port)

P3.2 INT0 (external interrupt)

P3.3 INT1 (external interrupt)

P3.4 T0 (Timer/Counter 0 external input)

P3.5 T1 (Timer/Counter 1 external input)

P3.6 WR (external Data Memory write strobe)

P3.7 RD (external Data Memory read strobe)

The alternate functions can only be activated if the corresponding bit latch in the port SFR contains a 1. Otherwise the port pin remains at 0.
I/O Configurations:

Figure shows a functional diagram of a typical bit latch and I/O buffer in each of the four ports. The bit latch (one bit in the port’s SFR) is represented as a Type D flip-flop, which will clock in a value from the internal bus in response to a “write to latch” signal from the CPU. The level of the port pin itself is placed on the internal bus in response to a “read pin” signal from the CPU. Some instructions that read a port activate the “read latch” signal, and others activate the “read pin” signal.

As shown in Figure 4, the output drivers of Port 0 and 2 are switch able to an internal ADDR and ADDR/DATA bus by an internal CONTROL signal for use in external memory accesses. During external memory accesses, the P2 SFR remains unchanged, but the P0 SFR gets 1s written to it. Also shown in Figure 4 is that if a P3 bit latch contains a 1, then the output level is controlled by the signal labeled “alternate output function.” The actual P3.X pin level is always available to the pin’s alternate input function, if any. Ports 1, 2, and 3 have internal pull-ups, and Port 0 has open drain outputs. Each I/O line can be independently used as an input or an output. (Port 0 and 2 may not be used as general purpose I/O when being used as the ADDR/DATA BUS for external memory during normal operation.) To be used as an input, the port bit latch must contain a 1, which turns off the output driver FET. Then, for Ports 1, 2, and 3, the pin is pulled high by a weak internal pull-up, and can be pulled low by an external source. Port 0 differs in that its internal pull-ups are not active during normal port operation. The pull-up FET in the P0 output driver is used only when the port is emitting 1s during external memory accesses. Otherwise the pull-up FET is off. Consequently P0 lines that are being used as output port lines are open drain. Writing a 1 to the bit latch leaves both output FETs off, so the pin floats. In that condition it can be used as
PREPAID ENERGY METER

a high-impedance input. Because Ports 1, 2, and 3 have fixed internal pull-ups, they are sometimes called “quasi bidirectional” ports. When configured as inputs they pull high and will source current (IIL, in the data sheets) when externally pulled low. Port 0, on the other hand, is considered “true” bidirectional, because when configured as an input it floats. All the port latches in the 80C51 have 1s written to them by the reset function. If a 0 is subsequently written to a port latch, it can be reconfigured as an input by writing a 1 to it.

Writing to a Port:

In the execution of an instruction that changes the value in a port latch, the new value arrives at the latch during S6P2 of the final cycle of the instruction. However, port latches are in fact sampled by their output Mbuffers only during Phase 1 of an clock period. (During Phase 2 the output buffer holds the value it saw during the previous Phase 1). Consequently, the new value in the port latch won’t actually appear at the output pin until the next Phase 1, which will be at S1P1 of the next machine cycle. If the change requires a 0-to-1 transition in Port 1, 2, or 3, an additional pull-up is turned on during S1P1 and S1P2 of the cycle in which the transition occurs. This is done to increase the transition speed. The extra pull-up can source about 100 times the current that the normal pull-up can. It should be noted that the internal pull-ups are field-effect transistors, not linear resistors. The pull-up arrangements are shown in the NMOS 8051 part, the fixed part of the pull-up is a depletion mode transistor with the gate wired to the source. This transistor will allow the pin to source about 0.25mA when shorted to ground. In parallel with the fixed pull-up is an enhancement mode transistor, which is activated during S1 whenever the port bit does a 0-to-1 transition. During this interval, if the port pin is shorted to ground, this extra transistor will allow the pin to
source an additional 30mA. In the CMOS 80C51, the pull-up consists of three pFETs. It should be noted that an n-channel FET (nFET) is turned on when a logical 1 is applied to its gate, and is turned off when a logical 0 is applied to its gate. A p-channel FET (pFET) is the opposite: it is on when its gate sees a 0, and off when its gate sees a 1. pFET1 in Figure 5 is the transistor that is turned on for 2 oscillator periods after a 0-to-1 transition in the port latch. While it’s on, it turns on pFET3 (a weak pull up), through the inverter. This inverter and pFET3 form a latch which holds the 1. Note that if the pin is emitting a 1, a negative glitch on the pin from some external source can turn off pFET3, causing the pin to go into a float state. pFET2 is a very weak pull up which is on whenever the nFET is off, in traditional CMOS style. It’s only about 1/10 the strength of pFET1. Its function is to restore a 1 to the pin in the event the pin had a 1 and lost it to a glitch.

**Port Loading and Interfacing:**

The output buffers of Ports 1, 2, and 3 can each drive 4 LS TTL inputs. These ports on NMOS versions can be driven in a normal manner by a TTL or NMOS circuit. Both NMOS and CMOS pins can be driven by open-collector and open-drain outputs, but note that 0-to-1 transitions will not be fast.

In the NMOS device, if the pin is driven by an open-collector output, a 0-to-1 transition will have to be driven by the relatively weak depletion mode FET in Figure 5a. In the CMOS device, an input 0 turns off pullup pFET3, leaving only the very weak pullup pFET2 to drive the transition. Port 0 output buffers can each drive 8 LS TTL inputs. They do, however, require external pull-ups to drive NMOS inputs, except when being used as the ADDRESS/DATA bus for external memory.
Pin Description:

VCC: Supply voltage.

GND: Ground.

Port 0:

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high impedance inputs. Port 0 can also be configured to be the multiplexed low order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1:

Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being
Pulled low will source current (IIL) because of the internal pullups. In addition, P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively, as shown in the following table. Port 1 also receives the low-order address bytes during Flash programming and verification.

<table>
<thead>
<tr>
<th>Port Pin</th>
<th>Alternate Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1.0</td>
<td>T2 (external count input to Timer/Counter 2), clock-out</td>
</tr>
<tr>
<td>P1.1</td>
<td>T2EX (Timer/Counter 2 capture/reload trigger and direction control)</td>
</tr>
<tr>
<td>P1.5</td>
<td>MOSI (used for In-System Programming)</td>
</tr>
<tr>
<td>P1.6</td>
<td>MISO (used for In-System Programming)</td>
</tr>
<tr>
<td>P1.7</td>
<td>SCK (used for In-System Programming)</td>
</tr>
</tbody>
</table>

**Port 2:**

Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (IIL) because of the internal pullups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that uses 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register. Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

**Port 3:**

Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the
internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (IIL) because of the pullups. Port 3 also serves the functions of various special features of the AT89S52, as shown in the following table. Port 3 also receives some control signals for Flash programming and verification.

<table>
<thead>
<tr>
<th>Port Pin</th>
<th>Alternate Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>P3.0</td>
<td>RXD (serial input port)</td>
</tr>
<tr>
<td>P3.1</td>
<td>TXD (serial output port)</td>
</tr>
<tr>
<td>P3.2</td>
<td>INT0 (external interrupt 0)</td>
</tr>
<tr>
<td>P3.3</td>
<td>INT1 (external interrupt 1)</td>
</tr>
<tr>
<td>P3.4</td>
<td>T0 (timer 0 external input)</td>
</tr>
<tr>
<td>P3.5</td>
<td>T1 (timer 1 external input)</td>
</tr>
<tr>
<td>P3.6</td>
<td>WR (external data memory write strobe)</td>
</tr>
<tr>
<td>P3.7</td>
<td>RD (external data memory read strobe)</td>
</tr>
</tbody>
</table>

**RST:**

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 96 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

**ALE/PROG:**

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory. If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly
pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

**PSEN:**

Program Store Enable (PSEN) is the read strobe to external program memory. When the AT89S52 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

**EA/VPP:**

External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset. EA should be strapped to VCC for internal program executions. This pin also receives the 12-volt programming enable voltage (VPP) during Flash programming.

**XTAL1:**

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

**XTAL2:**

Output from the inverting oscillator amplifier.

**ULN:**

- SEVEN DARLINGTONS PER PACKAGE.
- OUTPUT CURRENT 500mA PER DRIVER (600mA PEAK).
- OUTPUT VOLTAGE 50V.
- INTEGRATED SUPPRESSION DIODES FOR INDUCTIVE LOADS.
- OUTPUTS CAN BE PARALLELED FOR HIGHERCURRENT.
PREPAID ENERGY METER

- TTL/CMOS/PMOS/DTLCOMPATIBLE INPUTS.
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT.

DESCRIPTION:

The ULN2001A, ULN2002A, ULN2003 and ULN2004A are high voltage, high current Darlington arrays each containing seven open collector Darlington pairs with common emitters. Each channel rated at 500mA and can withstand peak currents of 600mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout. The four versions interface to all common logic families:

<table>
<thead>
<tr>
<th>ULN2001A</th>
<th>General Purpose, DTL, TTL, PMOS, CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>ULN2002A</td>
<td>14-25V PMOS</td>
</tr>
<tr>
<td>ULN2003A</td>
<td>5V TTL, CMOS</td>
</tr>
<tr>
<td>ULN2004A</td>
<td>6–15V CMOS, PMOS</td>
</tr>
</tbody>
</table>

These versatile devices are useful for driving a wide range of loads including solenoids, relays DC motors, LED displays filament lamps, thermal print heads and high power buffers. The ULN2001A/2002A/2003A and 2004A are supplied in 16 pin plastic DIP packages with a copper lead frame to reduce thermal resistance. They are available also in small outline package (SO-16) as ULN2001D/2002D/2003D/2004D.
What is a relay?

A relay is usually an electromechanical device that is actuated by an electrical current. The current flowing in one circuit causes the opening or closing of another circuit. Relays are like remote control switches and are used in many applications because of their relative simplicity, long life, and proven high reliability. Relays are used in a wide variety of applications throughout industry, such as in telephone exchanges, digital computers and automation systems. Highly sophisticated relays are utilized to protect electric power systems against trouble and power blackouts as well as to regulate and control the generation and distribution of power.
How relays work?

All relays contain a sensing unit, the electric coil, which is powered by AC or DC current. When the applied current or voltage exceeds a threshold value, the coil activates the armature, which operates either to close the open contacts or to open the closed contacts. When a power is supplied to the coil, it generates a magnetic force that actuates the switch mechanism. The magnetic force is, in effect, relaying the action from one circuit to another. The first circuit is called the control circuit; the second is called the load circuit.

Fig.: working of relay.

There are three basic functions of a relay:

1) On/Off Control,
2) Limit Control and
3) Logic Operation.

AT24C04, 4K SERIAL EEPROM:

The 4K is internally organized with 256 pages of 2 bytes each. Random word addressing Chip Number requires a 9-bit data word address.
Features

- Low-Voltage and Standard-Voltage Operation
  - 5.0 (VCC = 4.5V to 5.5V)
  - 2.7 (VCC = 2.7V to 5.5V)
  - 2.5 (VCC = 2.5V to 5.5V)
  - 1.8 (VCC = 1.8V to 5.5V)

- Internally Organized 128 x 8 (1K), 256 x 8 (2K), 512 x 8 (4K), 1024 x 8 (8K) or 2048 x 8 (16K)

- 2-Wire Serial Interface

- Schmitt Trigger, Filtered Inputs for Noise Suppression

- Bidirectional Data Transfer Protocol

- 100 kHz (1.8V, 2.5V, 2.7V) and 400 kHz (5V) Compatibility

- Write Protect Pin for Hardware Data Protection

- 8-Byte Page (1K, 2K), 16-Byte Page (4K, 8K, 16K) Write Modes

- Partial Page Writes Are Allowed

- Self-Timed Write Cycle (10 ms max)

- High Reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
  - ESD Protection: >3000V

- Automotive Grade and Extended Temperature Devices Available

- 8-Pin and 14-Pin JEDEC SOIC, 8-Pin PDIP, 8-Pin MSOP, and 8-Pin TSSOP Packages
Description:

The AT24C04 provides 4096 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 512 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C04 is available in space saving 8-pin PDIP, AT24C04 packages and is accessed via a 2-wire serial interface. In addition, the family is available in 2.5V (2.5V to 5.5V) version.

Device Operation

CLOCK and DATA TRANSITIONS:

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Data Validity timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION:

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition timing diagram).

STOP CONDITION:

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Start and Stop Definition timing diagram).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.
STANDBY MODE:

The AT24C01A/02/04/08/16 features a low power standby mode which is enabled: (a) upon powerup and (b) after the receipt of the STOP bit and the completion of any internal operations.

MEMORY RESET:

After an interruption in protocol, power loss or system reset, any 2-wire part can be reset by following these steps:

1. Clock up to 9 cycles.
2. Look for SDA high in each cycle while SCL is high.
3. Create a start condition as SDA is high.

Pin Configurations

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0 - A2</td>
<td>Address Inputs</td>
</tr>
<tr>
<td>SDA</td>
<td>Serial Data</td>
</tr>
<tr>
<td>SCL</td>
<td>Serial Clock Input</td>
</tr>
<tr>
<td>WP</td>
<td>Write Protect</td>
</tr>
<tr>
<td>NC</td>
<td>No Connect</td>
</tr>
</tbody>
</table>

Pin Description:

SERIAL CLOCK (SCL):

The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA):

The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-O Red with any number of other open-drain or open collector devices.
DEVICE/PAGE ADDRESSES (A2, A1, A0):
The A2, A1 and A0 pins are device address inputs that are hard wired for the AT24C01A and the AT24C02. As many as eight 1K/2K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section). The AT24C04 uses the A2 and A1 inputs for hard wire addressing and a total of four 4K devices may be addressed on a single bus system. The A0 pin is a no connect. The AT24C08 only uses the A2 input for hardwire addressing and a total of two 8K devices may be addressed on a single bus system. The A0 and A1 pins are no connects. The AT24C16 does not use the device address pins which limits the number of devices on a single bus to one. The A0, A1 and A2 pins are no connects.

WRITE PROTECT (WP):
The AT24C01A/02/04/16 has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect pin is connected to VCC, the write protection feature is enabled and operates as shown in the following table.

MAX232:-
- Operates With Single 5-V Power Supply
- LinBi CMOS Process Technology
- Two Drivers and Two Receivers
- 30-V Input Levels
- Low Supply Current . . . 8 mA Typical
- Meets or Exceeds TIA/EIA-232-F and ITU Recommendation V.28
- Designed to be Interchangeable with Maxim MAX232

ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015 Package Options
Include Plastic Small-Outline (D, DW) Packages and Standard Plastic (N) DIPs description.

The MAX232 device is a dual driver/receiver that includes a capacitive voltage generator to supply EIA-232 voltage levels from a single 5-V supply. Each receiver converts EIA-232 inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V and a typical hysteresis of 0.5 V, and can accept $\mu$30-V inputs. Each driver converts TTL/CMOS input levels into EIA-232 levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments L in ASIC library. The MAX232 is characterized for operation from 0°C to 70°C. The MAX232I is characterized for operation from –40°C to 85°C.

**D, DW, OR N PACKAGE**

(TOP VIEW)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>C1+</td>
</tr>
<tr>
<td>2</td>
<td>VS+</td>
</tr>
<tr>
<td>3</td>
<td>C1−</td>
</tr>
<tr>
<td>4</td>
<td>C2+</td>
</tr>
<tr>
<td>5</td>
<td>C2−</td>
</tr>
<tr>
<td>6</td>
<td>VS−</td>
</tr>
<tr>
<td>7</td>
<td>T2OUT</td>
</tr>
<tr>
<td>8</td>
<td>R2IN</td>
</tr>
<tr>
<td>9</td>
<td>R2OUT</td>
</tr>
<tr>
<td>10</td>
<td>T2IN</td>
</tr>
<tr>
<td>11</td>
<td>R1IN</td>
</tr>
<tr>
<td>12</td>
<td>T1OUT</td>
</tr>
<tr>
<td>13</td>
<td>R1IN</td>
</tr>
<tr>
<td>14</td>
<td>T1OUT</td>
</tr>
<tr>
<td>15</td>
<td>GND</td>
</tr>
<tr>
<td>16</td>
<td>VCC</td>
</tr>
</tbody>
</table>

**LCD**

**DESCRIPTION:**

- A 8051 (or derivate) is used to control the LCD.
- Needs decoded LCD-READ en LCD-WRITE signals, derived from controller signals AD00..AD07, A08..A15, /RD and /WR, to map the LCD into the external DATA area.
- Address line A00 is connected to the DEMULTIPLEXED controller signal AD00 and controls which LCD register is accessed.

- Data lines AD00..AD07 are directly connected to controller signals AD00..AD07.

- Control line 'BACKLIGHT' is used to switch the LED-backlight on (logic 1) or off (logic 0) or could be controlled from a PWM output.

---

**Fig.:** LCD interface with microcontroller.

---

<table>
<thead>
<tr>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
<th>12</th>
<th>13</th>
<th>14</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ground</td>
<td>VDD</td>
<td>Contrast</td>
<td>R/W</td>
<td>EN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Display Addresses:**

<table>
<thead>
<tr>
<th>A0</th>
<th>A1</th>
<th>A2</th>
<th>A3</th>
<th>A4</th>
<th>A5</th>
<th>A6</th>
<th>A7</th>
</tr>
</thead>
<tbody>
<tr>
<td>B0</td>
<td>B1</td>
<td>B2</td>
<td>B3</td>
<td>B4</td>
<td>B5</td>
<td>B6</td>
<td>B7</td>
</tr>
<tr>
<td>C0</td>
<td>C1</td>
<td>C2</td>
<td>C3</td>
<td>C4</td>
<td>C5</td>
<td>C6</td>
<td>C7</td>
</tr>
<tr>
<td>D0</td>
<td>D1</td>
<td>D2</td>
<td>D3</td>
<td>D4</td>
<td>D5</td>
<td>D6</td>
<td>D7</td>
</tr>
<tr>
<td>E0</td>
<td>E1</td>
<td>E2</td>
<td>E3</td>
<td>E4</td>
<td>E5</td>
<td>E6</td>
<td>E7</td>
</tr>
</tbody>
</table>
### Table 2.1., Pin assignment for <= 80 character displays

<table>
<thead>
<tr>
<th>Pin number</th>
<th>Symbol</th>
<th>Level</th>
<th>I/O</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Vss</td>
<td>-</td>
<td>-</td>
<td>Power supply (GND)</td>
</tr>
<tr>
<td>2</td>
<td>Vcc</td>
<td>-</td>
<td>-</td>
<td>Power supply (+5V)</td>
</tr>
<tr>
<td>3</td>
<td>Vee</td>
<td>0/1</td>
<td>I</td>
<td>Contrast adjust</td>
</tr>
<tr>
<td>4</td>
<td>RS</td>
<td>0/1</td>
<td>I</td>
<td>0 = Instruction input</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 = Data input</td>
</tr>
<tr>
<td>5</td>
<td>R/W</td>
<td>0/1</td>
<td>I</td>
<td>0 = Write to LCD module</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 = Read from LCD module</td>
</tr>
<tr>
<td>6</td>
<td>E</td>
<td>1, 1-&gt;0</td>
<td>I</td>
<td>Enable signal row 0 &amp; 1 (1st controller)</td>
</tr>
<tr>
<td>7</td>
<td>DB0</td>
<td>0/1</td>
<td>I/O</td>
<td>Data bus line 0 (LSB)</td>
</tr>
<tr>
<td>8</td>
<td>DB1</td>
<td>0/1</td>
<td>I/O</td>
<td>Data bus line 1</td>
</tr>
<tr>
<td>9</td>
<td>DB2</td>
<td>0/1</td>
<td>I/O</td>
<td>Data bus line 2</td>
</tr>
<tr>
<td>10</td>
<td>DB3</td>
<td>0/1</td>
<td>I/O</td>
<td>Data bus line 3</td>
</tr>
<tr>
<td>11</td>
<td>DB4</td>
<td>0/1</td>
<td>I/O</td>
<td>Data bus line 4</td>
</tr>
<tr>
<td>12</td>
<td>DB5</td>
<td>0/1</td>
<td>I/O</td>
<td>Data bus line 5</td>
</tr>
<tr>
<td>13</td>
<td>DB6</td>
<td>0/1</td>
<td>I/O</td>
<td>Data bus line 6</td>
</tr>
<tr>
<td>14</td>
<td>DB7</td>
<td>0/1</td>
<td>I/O</td>
<td>Data bus line 7 (MSB)</td>
</tr>
</tbody>
</table>

### Table 2.2., Pin assignment for > 80 character displays

<table>
<thead>
<tr>
<th>Pin number</th>
<th>Symbol</th>
<th>Level</th>
<th>I/O</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DB7</td>
<td>0/1</td>
<td>I/O</td>
<td>Data bus line 7 (MSB)</td>
</tr>
<tr>
<td>2</td>
<td>DB6</td>
<td>0/1</td>
<td>I/O</td>
<td>Data bus line 6</td>
</tr>
<tr>
<td>3</td>
<td>DB5</td>
<td>0/1</td>
<td>I/O</td>
<td>Data bus line 5</td>
</tr>
<tr>
<td>4</td>
<td>DB4</td>
<td>0/1</td>
<td>I/O</td>
<td>Data bus line 4</td>
</tr>
<tr>
<td>5</td>
<td>DB3</td>
<td>0/1</td>
<td>I/O</td>
<td>Data bus line 3</td>
</tr>
<tr>
<td>6</td>
<td>DB2</td>
<td>0/1</td>
<td>I/O</td>
<td>Data bus line 2</td>
</tr>
<tr>
<td>7</td>
<td>DB1</td>
<td>0/1</td>
<td>I/O</td>
<td>Data bus line 1</td>
</tr>
<tr>
<td>8</td>
<td>DB0</td>
<td>0/1</td>
<td>I/O</td>
<td>Data bus line 0 (LSB)</td>
</tr>
<tr>
<td>9</td>
<td>E1</td>
<td>1, 1-&gt;0</td>
<td>I</td>
<td>Enable signal row 0 &amp; 1 (1st controller)</td>
</tr>
<tr>
<td>10</td>
<td>R/W</td>
<td>0/1</td>
<td>I</td>
<td>0 = Write to LCD module</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 = Read from LCD module</td>
</tr>
<tr>
<td>11</td>
<td>RS</td>
<td>0/1</td>
<td>I</td>
<td>0 = Instruction input</td>
</tr>
</tbody>
</table>
Table 2.2. Pin assignment for > 80 character displays

<table>
<thead>
<tr>
<th>Pin number</th>
<th>Symbol</th>
<th>Level</th>
<th>I/O</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>Vee</td>
<td>-</td>
<td>-</td>
<td>1 = Data input</td>
</tr>
<tr>
<td>13</td>
<td>Vss</td>
<td>-</td>
<td>-</td>
<td>Contrast adjust</td>
</tr>
<tr>
<td>14</td>
<td>Vcc</td>
<td>-</td>
<td>-</td>
<td>Power supply (GND)</td>
</tr>
<tr>
<td>15</td>
<td>E2</td>
<td>1, 1-&gt;0</td>
<td>I</td>
<td>Power supply (+5V)</td>
</tr>
<tr>
<td>16</td>
<td>n.c.</td>
<td>-</td>
<td>-</td>
<td>Enable signal row 2 &amp; 3 (2\textsuperscript{nd} controller)</td>
</tr>
</tbody>
</table>

Instruction set:

Table 2.3. HD44780 instruction set

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Code</th>
<th>Description</th>
<th>Execution time**</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clear display</td>
<td>0 0 0 0 0 0 0 0 0 0 1</td>
<td>Clears display and returns cursor to the home position (address 0).</td>
<td>1.64mS</td>
</tr>
<tr>
<td>Cursor home</td>
<td>0 0 0 0 0 0 0 0 0 0 1 *</td>
<td>Returns cursor to home position (address 0). Also returns display being shifted to the original position. DDRAM contents remains unchanged.</td>
<td>1.64mS</td>
</tr>
<tr>
<td>Entry mode</td>
<td>0 0 0 0 0 0 0 0 1</td>
<td>Sets cursor</td>
<td>40uS</td>
</tr>
<tr>
<td>Instruction</td>
<td>Code</td>
<td>Description</td>
<td>Execution time**</td>
</tr>
<tr>
<td>----------------------</td>
<td>------</td>
<td>-----------------------------------------------------------------------------</td>
<td>------------------</td>
</tr>
<tr>
<td>set</td>
<td></td>
<td>move direction (I/D), specifies to shift the display (S). These operations are performed during data read/write.</td>
<td></td>
</tr>
<tr>
<td>Display On/Off control</td>
<td>0 0 0 0 0 0 1 D C B</td>
<td>Sets On/Off of all display (D), cursor On/Off (C) and blink of cursor position character (B).</td>
<td>40uS</td>
</tr>
<tr>
<td>Cursor/display shift</td>
<td>0 0 0 0 0 1 S/C R/L * *</td>
<td>Sets cursor-move or display-shift (S/C), shift direction (R/L). DDRAM contents remains unchanged.</td>
<td>40uS</td>
</tr>
<tr>
<td>Function set</td>
<td>0 0 0 0 1 DL N F * *</td>
<td>Sets interface data length (DL), number of display line (N) and character font (F).</td>
<td>40uS</td>
</tr>
<tr>
<td>Set CGRAM</td>
<td>0 0 0 1</td>
<td>CGRAM address</td>
<td>Sets the</td>
</tr>
</tbody>
</table>
### Table 2.3. HD44780 instruction set

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Code</th>
<th>Description</th>
<th>Execution time**</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address</td>
<td></td>
<td>CGRAM address. CGRAM data is sent and received after this setting.</td>
<td></td>
</tr>
<tr>
<td>Set DDRAM address</td>
<td>0 0 1</td>
<td>DDRAM address</td>
<td>40uS</td>
</tr>
<tr>
<td>Read busy-flag and address counter</td>
<td>0 1 BF</td>
<td>CGRAM / DDRAM address</td>
<td>0uS</td>
</tr>
<tr>
<td>Write to CGRAM or DDRAM</td>
<td>1 0</td>
<td>write data</td>
<td>40uS</td>
</tr>
<tr>
<td>Read from CGRAM or DDRAM</td>
<td>1 1</td>
<td>read data</td>
<td>40uS</td>
</tr>
</tbody>
</table>
Remarks:
- DDRAM = Display Data RAM.
- CGRAM = Character Generator RAM.
- DDRAM address corresponds to cursor position.
- * = Don't care.
- ** = Based on F_{osc} = 250kHz.

<table>
<thead>
<tr>
<th>Bit name</th>
<th>Setting / Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/D</td>
<td>0 = Decrement cursor position</td>
</tr>
<tr>
<td>S</td>
<td>0 = No display shift</td>
</tr>
<tr>
<td>D</td>
<td>0 = Display off</td>
</tr>
<tr>
<td>C</td>
<td>0 = Cursor off</td>
</tr>
<tr>
<td>B</td>
<td>0 = Cursor blink off</td>
</tr>
<tr>
<td>S/C</td>
<td>0 = Move cursor</td>
</tr>
<tr>
<td>R/L</td>
<td>0 = Shift left</td>
</tr>
<tr>
<td>DL</td>
<td>0 = 4-bit interface</td>
</tr>
<tr>
<td>N</td>
<td>0 = 1/8 or 1/11 Duty (1 line)</td>
</tr>
<tr>
<td>F</td>
<td>0 = 5x7 dots</td>
</tr>
<tr>
<td>BF</td>
<td>0 = Can accept instruction</td>
</tr>
</tbody>
</table>

Table 2.4. Bit names

2-line displays

Shown after reset (with N=1).

<table>
<thead>
<tr>
<th>Display size</th>
<th>Character positions</th>
<th>DDRAM addresses</th>
</tr>
</thead>
<tbody>
<tr>
<td>2*16</td>
<td>00..15</td>
<td>0x00..0x0F + 0x40..0x4F [1]</td>
</tr>
<tr>
<td>2*20</td>
<td>00..19</td>
<td>0x00..0x13 + 0x40..0x53</td>
</tr>
<tr>
<td>2*24</td>
<td>00..23</td>
<td>0x00..0x17 + 0x40..0x57</td>
</tr>
<tr>
<td>2*32</td>
<td>00..31</td>
<td>0x00..0x1F + 0x40..0x5F</td>
</tr>
<tr>
<td>2*40</td>
<td>00..39</td>
<td>0x00..0x27 + 0x40..0x67</td>
</tr>
</tbody>
</table>

Table 2.6. DDRAM address usage for a 2-line LCD
**KEYPAD:**

- It is used to interact with micro controller through user.
- Based on the application on embedded system has to provide with keypad to input data and or command.
- The all commands are given using the keypad like recharge amount and future application.

At the lowest level, keyboards are organized in a matrix of a row and columns The CPU accesses both rows and columns through ports; therefore, with two bit ports, an 4 X 4 matrix of keys can be connected to a microprocessor. When a key is pressed, a row and a column make contact; otherwise, there is no connection between rows and columns.

Figure shows a 4X4 matrix connected to two ports. The rows are connected to an output port and the columns are connected to an input port. If no key has been pressed, reading the input port will yield 1S for all columns since they are all connected to high (Vcc). If all the rows are grounded and a key is pressed, one of the columns will have 0 since the key pressed provides the path to ground. It is the function of the microcontroller to scan the keyboard continuously to detect and identify the key pressed.

**SOFTWARE:**

All the software is written in c language using the instruction set of 8051. the sequential flow of commands is as follows:

1. Initialise the mobile by sending the required AT commands trough the HyperTerminal software.
2. Continuously loop in the program to check whether any new SMS is received.

3. Read in the SMS, store it in the memory and give command to delete the SMS from the SMS memory in the mobile to keep index 1 for the next new SMS.

4. Check for the mobile number and the incoming SMS. If both are correct, display the SMS and time of arrival on the LCD.

5. According to the SMS, the respective LEDs glow. If any error occurs in the above procedure, display the error on the LCD and loop back.

In this s/w, we have written small subroutines, which make programming easy. Using the look-up table, we have stored all the responses for AT commands. All the interrupts, except those for serial communication, are masked.

**AT COMMAND SET:**

Similar to the modems, GSM cell phones accept the at command set only. The European telecommunications standard institute (ETSI) specifies this command set. According to the guidelines, commands should begin with the character string AT and end with “<CR>”. The input of a command is acknowledged by the display ‘OK’ or ‘ERROR’. A command currently in process is interrupted by each additional character entered. This means the next command should not be entered until we receive the acknowledgment. Otherwise the current command will be interrupted.
The commands supported are listed below:

**Mobile initialization commands**

1. ATE0: deactivate command echo
2. ATE1: active command echo
3. ATQ): display acknowledgements
4. ATQ1: suppress acknowledgements
5. ATV0.: output acknowledgement as numbers
6. ATV1.: output acknowledgement as text
7. AT+CGMM: issue manufacturers ID code
8. AT+CGMM: issue model ID code

**SMS related commands**

1. AT+CMGF: SMS format
2. AT+CMGL: List SMS
3. AT+CMGR: read in an SMS
4. AT+CMGD: delete an SMS in the SMS memory

Flowchart of program is shown in figure below
START

MODULE INITIALISATION

SERIAL PORT INITIALISATION

LCD INITIALISATION

IS MODULE INITIALISED

INIT.ERRO

CHECK FOR NEW THE SMS

IS MESSAGE NEW?

COMPARE THE INCOMING SMS WITH

IS PIN MATCHED

IS COMMAND MATCHED

DISPLAY THE SMS

SWITCH ON THE CONTROL

DELETE SMS AND KEEP INDEX EQUAL TO ONE

fig: flow chart of program
GLOBAL SYSTEM FOR MOBILE COMMUNICATION (GSM):

Why cellular system is used?

The number of customers wants the phone at every place like in car, in garden, during walk and everywhere.

- At first the cellular service is very expensive and time consuming and have very less numbers of channels, so the various development on cellular phones done.
- The development done three generation,

Architecture of GSM Network: -

![Diagram of GSM Network](image)

Figure 1. Layout of generic GSM network
GSM Network consists of three main parts:

- **Mobile Station (MS)** - carried by the subscriber.
- **Base Station Subsystem (BSS)** - controls radio link with mobile station.
- **Network & Switching Subsystem (NSS)** - mobility management and switching of calls between mobile users, and between mobile and fixed network users.

**Mobile Station Consists of:**

- Mobile Equipment (ME) such as hand portable and vehicle mounted unit
- Subscriber Identity Module (SIM), which contains the entire customer related information (identification, secret key for authentication, etc.)

**Base Station Subsystem Consists of:**

- Base Transceiver Station (BTS) defines a cell and is responsible for radio link protocols with the Mobile Station
- Base Station Controller (BSC) controls multiple BTSs and manages radio channel setup, and handovers. The BSC is the connection between the Mobile Station and Mobile Switching Center.

**Network and Switching Subsystems Consists of:**

- Mobile Switching Center (MSC) is the central component of the NSS. Operates all switching functions for the mobiles within its jurisdiction. Interface between mobile and other (including fixed) network. Its functions:
 Manages the location of mobiles
 Switches calls
 Manages Security features
 Controls handover between BSCs
 Resource management
 Interworks with and manages network databases
 Collects call billing data and sends to billing system
 Collects traffic statistics for performance monitoring
 Network Databases – Home Location Register and Visitor Location Register together
  with MSC provides the call routing and roaming capabilities of GSM.
 Home Location Register (HLR) contains all the subscriber information for the
  purposes of call control, and location determination. There is logically one HLR per
  GSM network, although it may be implemented as a distributed database.
 Visitors Location Register (VLR) is only a temporary storage while the particular
  subscriber is located in the geographical area controlled by the MSC/VLR. Contains
  only the necessary information provision of subscribed services.
 Authentication Center (AuC) is a protected database that stores the security
  information for each subscriber (a copy of the secret key stored in each SIM).
 Equipment Identity Register (EIR) is a list of all valid mobile equipment on the
  network.
Radio Link – Physical Layer: As we have mentioned above radio spectrum do all users share very limited resource. The method to divide up the bandwidth among as many users as possible, chosen by GSM, is a combination of Time- and Frequency-Division Multiple Access (TDMA/FDMA). FDMA divides frequency bandwidth of the (maximum) 25 MHz into 124 carrier frequencies. Each Base Station (BS) is assigned one or more carrier frequencies. Using a TDMA scheme each carrier frequency is divided in time, which forms logical channels. Time Division Multiple Access (TDMA) - the users take turns (in a round robin), each one periodically getting the entire bandwidth for a little burst of time. Frequency Division Multiple Access (FDMA) - the frequency spectrum is divided among the logical channels, with each user having exclusives possession of some frequency band. Mobile unit can be in two modes

- Idle - listening
- Dedicated – sending/receiving data

There are two kinds of channels: Traffic channels (TCH) carry speech and data traffic.

![Figure 2. Organization of bursts, TDMA frames, and multiframe for speech and data](image)
The fundamental unit of time in TDMA scheme is called a burst period and it lasts 15/26 msec. Eight burst periods are grouped in one TDMA frame (120/26 msec), which forms a basic unit of logical channels. One physical channel is one burst period per TDMA frame.

Traffic channels are defined as 26-frame multiframes. 26-frame multiframes lasts 120 msec (26 * 120/26). Out of 26 frames, 24 are for traffic, 1 is used for Slow Associated Control Channel (SACCH), and 1 is currently unused.

Network Aspects:

Figure 3. Signaling protocol structure in GSM

- Layer 1 is the physical layer.
- Layer 2 is the data link layer.
- Layer 3 is the GSM signaling protocol.
We have already seen structure used by physical layer, so we won’t expand it any more. Data
layer is modified version of some protocol used in ISDN and in Signaling System Number 7.
So the only interesting thing that is left for us is Layer 3 - GSM signaling protocol. Layer 3 is
itself divided into three sub-layers.

- Radio Resource Management
- Mobility Management
- Connection Management

Radio Resource Management (RR-Layer): -

The RR-Layer is concerned with the management of RR-session, which is the time that a
mobile is in dedicated mode, as well as the configuration of radio channels. In addition RR-
Layer manages power control, discontinues transmission and reception, and handovers.

Handover (handoff) is switching of an on-going call to a different channel or cell.

There are four types of handovers

- Switching channels in the same cell.
- Switching cells under control of the same Base Station Controller (BSC)
- Switching cells under the control of different BSCs, but belonging to the same Mobile
  service Switching Center (MSC)
- Switching cells under control of different MSCs.
The first two types of handover, called internal because they involve only BSC, and MSC is notified only on completion of the handover.

The last two types of handover, called external because they involve MSC.

Handover may be initiated by MSC (traffic balancing) or by mobile unit. The mobile unit always scans Broadcast Control Channel of up to 16 neighboring cells, and forms a list of the six best candidates for possible handover. This information is transmitted to current Base Station at least once per second. BSC and MSC use this information for handover algorithm.

One of the problems while making handover decision is whether the poor signal quality is due to physical interference or mobile having moved to another cell. There are two basic algorithms for making handover decision:

- **Minimum acceptable performance.** If signal degrades beyond some point, then transmission power is increased. If power increase does not lead to improve then handover is performed. Disadvantages: increasing transmission power may cause interference with neighbor cell.

- **Power budget.** Uses handover to improve transmission quality in the same or lower power level. This method avoids neighbor cell interference, but is quite complicated.
Server Side: -

Server side is nothing but powerhouse control room. At which all energy Meters are controlling, updating, and monitoring.

Server:-

In the simplest of terms, one can imagine a company’s information system as consisting of one or more database and some number of employees who need to access them remotely. In this model, the data are stored on powerful computer called “SERVER”.

Server Side Module has two main parts,

1) **GSM MODULE**

2) **SERVER PC (CONTROL UNIT)**

**GSM MODULE:**

- The GSM model is used for transition purpose
- It interconnect the server pc and meter as well as GSM based cell phones
- When there is request from GSM model accepts it and forward to PC for updating and processing
- The updated requests and processed
- Request_Are_Taken_From_Server pc and transmitted to the GSM based devices i.e. mobile and meter
The GSM module we used is GSM 8

**Fig: GSM-8 MODULE.**

**AutoLog® GSM- 8:**

GSM-8 is new model. GSM-8 will be released in the 1st half of year 2006. Build-in GSM modem. One free serial port (other serial port is used by modem), which supports AutoLog® Serial Plug-in modules.

AutoLog® GSM-RTU devices are designed especially to be used in applications where GSM communication is needed. Programming is made very easy; build-in GSM driver handles all the complex GSM communication tasks automatically so user can concentrate on application programming. AutoLog® GSM-RTU can be
programmed locally using a cable or remotely through GSM network using PC based programming tool or just GSM phone.  

**Technical Features:**

<table>
<thead>
<tr>
<th>Feature</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital inputs (DI)</td>
<td>4 pcs&lt;br&gt;12/24 VDC / max. 8 mA / PNP / opto-isolated</td>
</tr>
<tr>
<td>Digital outputs (DO)</td>
<td>2 pcs&lt;br&gt;12/24VDC / max. 2 A / NPN / opto-isolated</td>
</tr>
<tr>
<td>GSM/GPRS modem</td>
<td>Integrated GSM/GPRS modem and driver.</td>
</tr>
<tr>
<td>GSM/SMS communication</td>
<td>GSM-RTU use SMS -messages to communicate bidirectionally with SCADA, GSM phone or other GSM-RTUs. SMS -messages can be used to transfer measurement reports and logs, alarms, events, controls, settings, acknowledging and remote programming of GSM-RTU.</td>
</tr>
<tr>
<td>GPRS/FTP communication</td>
<td>GSM-RTU use GPRS/FTP for sending measurement reports and logs to SCADA.</td>
</tr>
<tr>
<td>Call controls</td>
<td>Special controls can be made using free of charge incoming call phone number identification.</td>
</tr>
<tr>
<td>I²C Port</td>
<td>1 pcs&lt;br&gt;HMI, iButton, etc.</td>
</tr>
<tr>
<td>HMI -user interface</td>
<td>Local user interface can be connected through I²C-port</td>
</tr>
</tbody>
</table>
## PREPAID ENERGY METER

<table>
<thead>
<tr>
<th>Feature</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Battery backup</td>
<td>Yes</td>
</tr>
<tr>
<td>Application program capacity</td>
<td>512kB FLASH, 8000 programming lines (FLASH), 256 programming lines, one line is 160 characters and can handle many commands. In addition it has 240 numbers memory for incoming phone number identification and 256 table rows for time controls and 256 -iButton identification.</td>
</tr>
<tr>
<td>Programming tool (PC)</td>
<td>AutoLog® GSMProgrammer</td>
</tr>
<tr>
<td>PID controllers</td>
<td>32 build-in PID controllers</td>
</tr>
<tr>
<td>Size (w x h x d)</td>
<td>190 x 125 x 65 mm</td>
</tr>
<tr>
<td>Weight</td>
<td>~0,3 kg</td>
</tr>
<tr>
<td>Operating temperature**</td>
<td>-20...+55 °C</td>
</tr>
<tr>
<td>Storage temperature**</td>
<td>-30...+85 °C</td>
</tr>
<tr>
<td>Power supply</td>
<td>12 / 24VDC or 10/18VAC max. 5VA</td>
</tr>
</tbody>
</table>
The control unit is placed at base station OR mobile switching center.

The database consisting in the server sides are information about the customer authority, ID, IP-address.

The programmable OR charging data base is updated as per consumption of power by customer

The server provides customer account with user password to provide security.

The GSM model connected with server is connecting unit between GSM devices live GSM model and GSM meter

It accepts regular information at particular time from each meter in network.

The meter sends reducing units and the server accepts it and updated the internal updates

The information updates that the server reduce the unit as per reduced at particular meter.
➢ The server also responsible per recharge the meter.

➢ When any meter request for units OR balance by sending 16-bit data to server address that units in database of that particular meter and also send to meter for display it for user convenient

➢ As one unit consumed by user the meter sends the message to reduce the unit and server updates the databases that particular meter.

➢ The various S/w are used at server side for the above application.

➢ The balance enquiry is also done through the GSM based mobile.

➢ The user has to request and the S/w makes record for that particular GSM Phones like it ID, authorization of IP address

➢ After checking balance the server send response to that particular meter.

➢ The balance is also recharge through meter OR GSM mobiles

➢ The database include balance/unit list per various balance of 16-bit number such like

<table>
<thead>
<tr>
<th>Balance/unit</th>
<th>P.I.N.code</th>
</tr>
</thead>
<tbody>
<tr>
<td>300/600</td>
<td>1234 5678 9876 6785</td>
</tr>
<tr>
<td>*</td>
<td>*</td>
</tr>
<tr>
<td>*</td>
<td>*</td>
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<tr>
<td>*</td>
<td>*</td>
</tr>
<tr>
<td>*</td>
<td>*</td>
</tr>
<tr>
<td>1000/2000</td>
<td>3456 4356 7685 9807</td>
</tr>
</tbody>
</table>

Fig: Table shows the Balance (Rs)/Unit and its P.I.N. code.

➢ Such a way all data base for balance/ data is fielded.
PREPAID ENERGY METER

➢ When one number is used that will deleted from database and new number is entered for that unit of balance.

➢ The pin number provided to customer, which it pay for that card sold at stores as per the cell phone services.

ADVANTAGES:

• Overdue.

• Electricity piracy.

• User friendly.

• Prepaid billing gives facility of direct paying via meter or GSM mobile.

• Also through GSM mobile user have facility of balance enquiry.

• Useful for avoid corruption.

• Single control from server make whole system monitoring and security.

• Useful for easy billing of electricity.

• Less man power is used.

• Disconnect /reconnect cost reduced by 90%.

• Easy to maintain.

• Time saving.

• Gives the door to door facility.

FUTURISTIC:

Easy to recharge by using GSM mobile phone also.

Any new scheme of electricity office can be display on GSM mobile phone.
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   WSE WILEY Edition by Yi-Bing Lin & Imrich Chlamate.

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3) www.Projectguide.com
DEVELOPMENT OF GSM BASED EMBEDDED SYSTEM

FOR

PREPAID ENERGY METER.

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