Programmable Logic Devices Architecture.
The familiarity with PLD architecture facilitates the designer to select an appropriate device, which best suits his application.

The features of PLD’s greatly affects the design considerations due to their architecture and Configuration characteristics.
The Intention of this module.

Fare background of synthesis will help the designer for the selection of the appropriate device depending on the size and complexity of the design.

By knowing the details of the internal available logic, designer can judge which part of the design will fit into the device and which will not.
Why to go for PLD’s?

• Flexibility.
• In system programmability.
• Less project development time.
• Best prototyping solution.
• Cost effective solutions.
• Involves less risk.
• Design security.
• Consumes less board area.
• Reconfigurable computing.
• Best suits hardware verification for design.
The general structure of PLD’s

- Any PLD consists of following blocks.
  - **Configurable Logic.**
    - Flip-flop.
    - Combinational Logic.
    - Embedded logic.
  - **Programmable Interconnects.**
    - Connects internal logic as well as input output blocks.
  - **Input Output Blocks.**
    - Communicates with external signal ,by programmable i/o facilities.
Programmable Logic

Configuration Memory

Bit Stream

Interconnect Switch

User control
Figuer comes here
Down-load Cable

VHDL or Verilog Code
Device independent

Device Type, constraints

Gate Level circuit
Device Type, constraints
FloorPlanning

User Constraint file

Software

Design entry
Synthesis
Implementation
Bit stream

Configurable Logic.

Configurable Switch Matrix.

Configuration Memory

PLD chip

LUT’s or Gates
Flip-Flops

Transistor switch
Muxes

Volatile
Non-volatile.

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The general structure of PLD’s

- **Configuration memory.**
  - It is the heart of PLD.
  - Configuring a PLD means, changing the contents of configuration memory – by downloading bit stream.
  - Configuration memory contains the status of programmable switches, which will form the logic. (Either ON or OFF)
  - Vendor software produces device specific bit-stream according to the user design and constraints.
Other side of the coin.

- We have to pay the price for all the extra advantages we are getting from PLD’s.
- The programmable interconnects consumes most of the die area, more than the ASIC for the same functionality.
- Operating speed is less than ASIC, for the same functionality due to added interconnect delays in the path.
Delays in the path.

Connection Established.  Equivalent circuit.

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Classification of the PLD’s.

- PLD’s are mainly classified considering the following :-
  - Logic Density and complexity
    - Numbers of usable gates and Flip-flops.
  - Basic Architecture.
    - Look-up table or PAL based.
  - Configuration Memory type .
    - Volatile or non volatile.
Classification of PLD’s

Programmable Logic.

Simple PLDs
- EPROM
- EEPROM
- FLASH

Complex PLDs
- CPLD
  - EPROM
  - EEPROM
  - FLASH
- FPGA
  - SRAM
  - Antifuse

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Importance of the Memory technology in PLD’s

- Following factors are related to the configuration memory type.
  - Programming speed.
    - Decides the time for configuration.
  - Amount of Die area consumed per unit cell.
    - Decides the logic density per sq. cm.
  - Volatile or Non volatile.
    - Decides whether to use of external non-volatile memory.
Simple Programmable Logic Devices . (SPLD’s)

- PAL like structure.
  - Consists of an AND and OR array.
  - AND array realizes selected product terms.
  - OR array OR’s together the product terms.
  - SPLD’s contain limited number of Flip-Flops.

- Size of the AND-OR array can not be increased beyond certain limit , due to limitation of current buffers , driving the array inputs.

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High Capacity Programmable Logic Devices

Segmented Interconnects.

Continuous Interconnect.

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High Capacity Programmable Logic Devices

- Complex Programmable Logic Devices.
  - Also called as EPLD, PEEL, MAX by diff. Vendors.
  - Non volatile, PROM based devices.
  - Having a structure with 2 to 64 PAL like structures, each containing one Flip-Flop.
  - Have continuous interconnect structure, so delays are predictable.
  - Having types which uses configuration memory types like EPROM, EEPROM, FLASH.

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Field Programmable Gate Arrays (FPGA’s).

- **Two types depending on the type of configuration memory:**
  - SRAM based, volatile.
  - Antifuse, nonvolatile (one time programmable).

- **Further can be divided according to Granularity as**
  - Fine Grained.
  - Coarse Grained.
FPGA - SRAM Based.

- Configuration memory is of type Static RAM, which is volatile.
- Requires external non-volatile memory to store the bit-stream due to the volatile nature of internal configuration memory.
- Incorporates look up tables in logic blocks to implement combinational functionality, with flip-flops.
- Logic blocks are arranged in the form of arrays surrounded by interconnect and I/O blocks.
FPGA – Antifuse.

- One time programmable FPGA’s, non-volatile in nature.
- Switches used are of Antifuse type.
- Connection is established by flowing the particular amount of current through the Antifuse switches, to fuse them.
- The fuse blows due to the programming current and converts to low resistance element (100 \( \Omega \)) from (\( \sim 5 \, M\Omega \)) in a programmer called as activator.
- e.g. Actel antifuse devices uses the PLICE technology i.e (Programmable Low Impedance Circuit Element.)
FPGA – Antifuse.

- Radiation Hardened devices, so used in space applications and other similar situations where radiations are predominant and may lead to device erasure.
- Occupies less die area than SRAM based FPGA’s due to small size of configuration memory, so logic density is high for the same die area.
Anti-fuse FPGA’s

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Granularity of FPGA’s.

- Granularity of FPGA means - the lowest level of available logic upto which the user can have direct control.
- There are three types of structures.
  - Fine grained structure.
    - Logic available is in form of gates and flip-flops
    - Higher flexibility at the cost of enormous burden on the interconnect structure.
    - Delays incurred in the signal path are more.
Granularity of FPGA.

- **Coarse Grained structure.**
  - Fixed high performance functional units are available instead of logic gates. e.g. Functional units like ALU, Counters are present.
  - Flexibility is lost [to some extent] but, burden on interconnect structure is reduced by high degree.
  - High performance due to reduced interconnect path delays.
Granularity of FPGA.

- **Mixed Grained Architecture.**
  - By combining the advantages of both fine and coarsed grained architectures, it balances features like, flexibility and high performance.
  - Few high performance blocks with logic gates and flip-flops are incorporated.
  - e.g Xilinx Spartan II architecture.
    All QuickLogic family Devices.
Programmable Logic Market share.

- Xilinx
- Altera
- Cypress
- Lattice
- Cirrus Logic
- Quick Logic
- Actel
- Atmel
- Lucent

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Evaluation of performance PLD’s.

PREP (Programmable Electronics Performance Company.)

- It’s function is to provide standard means to benchmark, compare and analyze CPLD and FPGA architecture from different vendors.
- PREP has defined certain set of circuits, which, each vendor has to implement in his PLD and send the implementation reports to PREP.
- PREP collects, verifies and publishes vendor data which facilitates the engineer to determine which CPLD or FPGA best suits his application.
Xilinx 9500 CPLD Architecture.

MAJOR BLOCKS ARE,

- **Function blocks** (i.e Configurable Logic.) Consists of smaller blocks each having PAL like structure and a Flip-flop, called as Macrocell.
- **Input output blocks**: Incorporates several configurable features with diff. I/O standards to facilitate proper input output of signals, depending on the design and board conditions.
- **Interconnect switch matrix**: Connects internal logic as well as their connection with I/O blocks.
- **Global Pins**: Have special routing and buffers associated with them. These have better driving capability, to maintain the proper timing instances of the attached signals.
- **JTAG Interface**: Interface used for boundary scan as well as programming.
Function block.
Xilinx 9500 CPLD Architecture.

- DETAILS OF FUNCTION BLOCK.
  - Consists of several macrocells (18 for this architecture.)
  - 36 inputs (for xc9500) and 54 inputs (for xc9500xv) are coming from switch matrix to the function block.
  - All these variables are available in direct as well as complemented form, for each macrocell.
  - Product term allocator is available with each macrocell and will allocate the product terms to the macrocells.
  - Each macrocell output is connected to one of the I/O block, as well as fed back to the interconnect switch matrix to use it as input for other internal logic block.
Xilinx 9500 CPLD Architecture.

- DETAILS OF MACROCELLS.
  - Each parameter of the flip-flop is configurable. Two options for clock and Set /Reset :- Global or Product Term.
  - 5 AND Gates are available with each macrocell.
  - Up-to 90 product terms can be combined in single macrocell from the other macrocells within the same function block using product term allocators ,with maximum incremental delay of 8*tPTA.
  - Product term allocator uses some product terms to use as control signals within that macrocell.
  - SOP form output can be Bypassed,Latched,inverted or conditionally inverted according to requirement.
Product term allocator.
Product term can be used as direct control term.

Product term can be given to other macrocells.

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How to combine product terms ??????

10 product terms

15 product terms

5 product terms.

5 product terms.

5 product terms.

5 product terms.

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GLOBAL SIGNALS.

- Three Global signals are available:
  - Global clock, Global Set/reset, Global Tri-state
- The use of these signals:
  - Minimize signal skew, thus retains the time instance.
  - Maintains the shape of the signal.
  - Routes critical nets.
  - Reduce routing congestion.
  - Are used to implement high speed I/o interface.
Xilinx 9500 CPLD Architecture

- **INPUT-OUTPUT BLOCK.**
  - Clamp diodes are provided to protect the chip from excessive positive and negative voltage.
  - Programmable pull-up and pull-down are provided to tie the package pin to either logic ‘1’ or ‘0’, so that unused pins can be connected to the known state.
  - Slew rate control is used to change the rise time of the switching signal to reduce the switching noise while transition.
  - Tri-state Buffer control can be connected either to product term enable (PTOE) or Global tri-state control pins.
Macrocell

To FastCONNECT
Switch Matrix

((Inversion in
AND-array))
Product Term OE
PTOE

OUT

To other
Macrocells

I/O Block

V_CCINT

V_CCIO

Pull-up
Resistor*

User-
Programmable
Ground

Slew Rate
Control

* Pull-up resistors are used to prevent floating pins during programming and other times. They are disabled during normal operations.

Available in
XC95216
and XC95288

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Timing Model for the CPLD.

Points to be noted in case of CPLD.

- 9500 series CPLD’s have only 5 timing paths. This is possible because the signal can travel only one of these 5-paths, when going from input to output.
- signal travels is almost always similar and the continuous structure of the CPLD interconnect structure.
- The delays of these timing paths are fixed. [ and are given in the data-sheet ].
- Hence these delays are predictable
- Therefore the performance of CPLD based designs is predictable.
Why Cool Runner runs cool?

- Conventional PLD’s uses wired- and logic to implement the product terms. These are area efficient, but slow.
- To cure the problem, conventional PLD’s uses bipolar sense amplifiers to improve speed.
  Sense Amplifiers are a special class of analog circuits which improve the speed of a wired-and product term output, by sensing a small change at the input. (50 mV.)
- The use of bi-polar circuit [sense amplifier] per product term increases the Static power consumption, leading to increase in total device power consumption.
Why Cool Runner runs cool?

- By replacing the conventional sense amplifier methods with the cascaded chain of pure CMOS gates, dynamic power consumption is reduced.
- Due to the absence of bipolar circuits, and the use of pure CMOS methods, these devices consumes very low power.
- Thus best suits the situations, where availability of power is at premium.
Architecture of the Cool Runner.

- XPLA3 architecture consists of three major blocks:
  - **Logic block** – No. depends on the device capacity. Each one contains 16 macrocells.
  - **ZIA** – Zero-power Interconnect Array. 36 lines go from ZIA to each logic block.
  - **I/O blocks** – Connect the internal logic to the outside world through ZIA.

- 36 pairs of true and complement inputs from the ZIA feed the 48 product terms in each of the logic block.
Logic block of XPLA3 architecture

- Within the 48 P-terms there are 8 control terms LCT[0:7] available as control inputs to each macrocell for use as Asynchronous clocks, Resets, Presets and output enables.
- PT0 to PT7 are available as local control terms.
- PT8 to PT15 are used for Fold-back Nand logic.
- PT16 to PT31 goes individually to each macrocell.
- PT32 to PT47 are available as Product term clocks.
- All the product terms are available for each programmable OR gate associated with each of the 16 macrocells.
Logic block of XPLA3 architecture.

- Fold-back Nands are used to effectively increase the product term width.
- This structure provides inverted product term as an input to all other product terms.
- The VFM (variable Function multiplexer) is used to increase the logic optimization by implementing the any two input logic function before entering the macrocell.
- If the macrocell needs extra product terms, it simply gets the additional product terms from the array as being a PLA type structure (advantage over 9500 series, in which extra product terms include additional delay of Product Term Allocator.)
Macrocell of XPLA3 architecture

- Macrocell register can be configured as either level or edge triggered, D / T flip flop.
- Flip-Flops can be driven by one of the eight sources. (Global or Product term clock.)
- Two feedback paths are given to the ZIA, one from macrocell and one from I/O block.
- Logic implemented in the buried macrocells can be fed back to the ZIA via the macrocell path.
Input Output block.

- Output enable has eight possible modes.

- Have the facility of programmable pull up or pull down, eliminating need of external termination.

- I/o are 5V Tolerant and has single bit slew rate control to reduce the EMI generation.
XILINX FPGA’s

- XC4000 series
- Virtex series
- Spartan Series
Major Blocks in XC4000 series

Three major blocks present:

- **Configurable Logic Blocks i.e. CLB’s**
  Core logic is present in this block.

- **Input Output Blocks i.e. IOBs**
  Provides interface between core logic and package pins.

- **Programmable Interconnect Interface.**
  Connects the logic as well as I/Os with several I/O standards.
Configurable Logic Block - CLB.

- The Core logic of FPGA is in this block.
- Includes two 4-i/p & one 3-i/p Look-up tables [LUT].
- These LUT’s can be used to implement combinational logic [max. up to 9 variables] by either combining them or using them independently.
- LUTs can also be used as in 16*1, 16*2 or 32*1 RAM.
- Two storage elements are present and can be used as D / T flip-flop with configurable clock.
- Flip-flop can have, either Set or Reset. [Not both].
The internals of LUTs.

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Configurable Logic Block.

- LUTs can also be used as RAM, DPRAM, ROM.
- Total four outputs are available out of which two are direct outputs and two are latched outputs coming from the two storage elements.
- The LUTs contains dedicated arithmetic logic for fast generation of carry and borrow signals, [useful in DSP applications].
- Combinational logic and Flip-flops can be used independently, [due to presence of multiple input to output paths], which leads to effective device utilization. [which was not the case in XC9500 series CPLDs.]
Dedicated Arithmetic Logic for fast carry and borrow generation.
Input Output block.

- Input signals also connect to an input register that can be programmed as either an edge-triggered flip-flop or a level-sensitive latch.
- Output signals can pass directly to the pad or be stored in an edge-triggered flip-flop.
- Programmable pull-up and pull-down resistors are useful for tying unused pins to Vcc or ground to minimize power consumption and reduce noise sensitivity. [WHY / HOW ??]
- Separate clock signals are provided for input and output flip-flops.
Input output block
Interconnect structure.

- Interconnect structure is hierarchical.
- Interconnect structure is segmented in nature.
- Hierarchy is used to
  - To reduce path delays.
  - Save routing resources from intermediate channels.
  - Reduce number of configuration bits, while retaining good performance.
- As I/Os are not permanently connected to logic blocks. Hence full flexibility is available for pin locking.
Interconnect structure for XC4000 FPGAs

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Interconnect structure.
Interconnect structure.
There are different kind of interconnects with different lengths.
- General purpose interconnects.
- Double length lines.
- Triple length and such up to octal length lines.
- Direct interconnects.
- Long lines.

I/O blocks can communicate with internal interconnect structure through Versa-Ring surrounding the internal logic and interconnects.
Interconnects.

Programmable interconnect point.

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Architectural Resources in FPGA.

- Architectural resources are extra features available in any device.
- These are standard data path blocks, which are the essential parts of any design. e.g. wide function decoders, memory-blocks, arithmetic operation blocks.
- Use of Architectural resources saves the internal logic resources and gives high performance.
Architectural Resources in FPGA

• Tri-state Buffers.
• A pair of tri-state buffers is associated with each CLB in the array.
• They can therefore be used to implement multiplexed or bi-directional buses on the horizontal long lines, saving logic resources.
• Programmable pull-up resistors attached to these longlines help to implement a wide wired AND function.
Architectural Resources in FPGA

- Wide Edge decoders
  - Dedicated decoder circuitry boosts the performance of the large decoding function.
  - This is implemented by using wired AND logic.

- Four programmable decoders are located on each edge. Decoder outputs can be combined or made available outside.
Architectural Resources in FPGA

- On chip clock
What is Configuration?

- Configuration is the process of,
  - Loading design specific programming data into one or more FPGAs
  - To define the functional operation of the internal blocks and their interconnections
Special purpose pins used for Configuration

- There are three types of pins in XC4000 Series Devices
  - Dedicated pins
  - Special function User I/O pins
  - Unrestricted user programmable I/O pins
Dedicated Pins

- **CCLK** - Acts as a Configuration clock. Internal oscillator generates CCLK. CCLK is selected as 1MHz (default) or 8MHz.

- **DONE** - Is a bi-directional signal and as an output indicates completion of configuration process.

- **PROGRAM** – Clears FPGA configuration memory and initiates the configuration cycle.

- **VCC** - Eight or more connections to nominal 5V supply.

- **GND** - Eight or more connections to ground.

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Special Function User I/O pins

- **M0, M1, M2**
  Used for configuration mode selection. These pins are sampled at Power-On to determine the configuration mode to be used.

- **INIT**
  Is a Bi-directional signal used to delay the configuration. A LOW on this pin during configuration indicates that a configuration data error has occurred.

- **A0 to A17**
  During Master Parallel configuration these pins address the configuration EPROM.
Special Function User I/O pins

- **D0 – D7**
  During Master Parallel and Peripheral modes these pins receive configuration data.

- **DIN**
  Is the Serial configuration data input that receives data on the rising edge of CCLK.

- **DOUT**
  Is the serial configuration data output. In daisy chaining acts as a DIN for next FPGA in chain.

- **TDI, TDO, TMS, TCK**
  Pins are used for Boundary Scanning.
User-Programmable I/O Pins

- Special Function User I/O pins can be used as user programmable I/Os after configuration.

- Before and during configuration, outputs, not used for configuration process are tri-stated with a 50K-100K Pull-up resistor.

- After configuration if an IOB is unused it is configured as an input with a 50K-100K Pull up resistor.
Configuration modes

- There are six configuration modes.
- These modes are selected by M0, M1 and M2 pins.

<table>
<thead>
<tr>
<th>Mode</th>
<th>M2</th>
<th>M1</th>
<th>M0</th>
<th>CCLK</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>Master Serial</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>output</td>
<td>Bit-Serial</td>
</tr>
<tr>
<td>Slave Serial</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>input</td>
<td>Bit-Serial</td>
</tr>
<tr>
<td>Master Parallel Up</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>output</td>
<td>Byte-Wide, increment from 00000</td>
</tr>
<tr>
<td>Master Parallel Down</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>output</td>
<td>Byte-Wide, decrement from 3FFFFF</td>
</tr>
<tr>
<td>Peripheral Synchronous*</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>input</td>
<td>Byte-Wide</td>
</tr>
<tr>
<td>Peripheral Asynchronous</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>output</td>
<td>Byte-Wide</td>
</tr>
<tr>
<td>Express</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>input</td>
<td>Byte-Wide</td>
</tr>
<tr>
<td>Reserved</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>
Slave Serial Mode

- Is default mode when mode pins are left unconnected
- Device accepts serial data on rising edge of CCLK
Master/Slave Serial Mode

NOTE:
M2, M1, M0 can be shorted to Ground if not used as I/O

NOTE:
M2, M1, M0 can be shorted to VCC if not used as I/O

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Master Modes

- Master modes use an internal oscillator to generate Configuration Clock (CCLK) for driving potential slave devices
  - CCLK is by default 1MHz

- There are 3 Master modes,
  - **Master Parallel Up/Down**: Generate the CCLK signal and PROM addresses and receive byte parallel data
    - Starting address can be either 0 or 3FFF depending on selection of up/down mode
  - **Master Serial**: Generates CCLK and receives configuration data serially from a serial PROM
Master Parallel Mode.
Synchronous Peripheral Mode

- This mode can also be considered as Slave Parallel Mode
- An external signal drives the CCLK input of FPGA
- RDY/BUSY acts as an acknowledge signal and is useful for test purposes

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Asynchronous Peripheral Mode

- This mode uses the trailing edge of the logic AND condition of WS and CS0 being low and RS and CS1 being high to accept data from a microprocessor bus.
- RDY/BUSY signal acts as a handshake signal to the microprocessor.
Virtex Architecture.

- Virtex architecture contains following blocks.
  - CLBs.
  - Versa-Ring.
  - Block RAMs.
  - IOBs.
  - DLLs.
Virtex Architecture.

- One CLB consists of two slices.
- One slice contains:
  - Two 4 input LUTs
  - Two flip-flops.
  - Carry Logic associated with the logic.

[does this sound familiar]
Virtex Routing

- There are two parts in the interconnect structure.
  - **Versa Block**
    - This block contains CLB local feed-backs, direct connections between the adjacent CLBs, the connections to the GRM (General Routing Matrix).
  - **GRM**
    - Mainframe routing throughout the chip.
    - Communicates between Versa-Blocks.
Virtex interconnection strategy.

- As chip complexity and density goes on increasing the interconnection strategies have to be efficient enough to route the signals effectively with the minimal delays in the path.
- Virtex architecture is designed considering these factors.
- The interconnection is done by the router in such a way that it will always first try the local interconnects for routing as far as possible and then only will go through the GRM. This strategy minimizes routing delays.
QuickLogic’s Expanding Families of ESPs & FPGAs
The limitations of using the soft IP cores

- Mapping a complex soft IP function in the PLD often presents enormous challenges from the standpoint of performance, timing considerations, size, silicon cost, routability and pin stability.
- It may also affect the performance of the other functionality in same PLD in SOC kind of applications.
- Requires the continuous technical support from vendor, licensing formalities etc.
The Quick-Logic approach.

- The QuickLogic uses the ESP i.e (Embedded Standard Product) approach in which fixed high performance units are embedded within the conventional programmable logic cells.
- The best example of mixed Grained Architecture.
- An ESP includes three major parts :-
  - Programmable logic Array.
  - An embedded standard function.
  - Interface communicating with standard function and the programmable logic.
- In order to support the ESP the silicon technology must support the features like high density and low impedance routing resources, to achieve high combined performance.
The Quick-Logic approach.

- QuickLogic uses high performance silicon technology which provides the high density as well as high performance, patented as Via-Link technology.
- Via-Link connections are extremely small and are placed in the metal layers of the device, instead of placing them on the bottom silicon layer. [remember slide –6]
- Thus saving die space, reducing cost and attaining full routability with high performance due to reduced connection lengths.
The Via-Link technology.

- The Via-Link element is formed by depositing a very high resistance layer (>1 Gohm) of amorphous silicon above a tungsten Via plug which will act as programming element.
- When programming voltage is applied across the via, silicon converts to low resistance state (Typically 30 ohm), forming permanent metal–metal connection. (Non Volatile)
  [note: pure Si is an insulator ]
- As these Via-links are placed in between the metal interconnects, effectively they do not consume silicon die area, saving die space.
The Via-Link technology.

FIGURE 4. Four Layer Metal ViaLink® Structure

Actual Via-Link
QuickDSP Architecture.

- Combines high-speed dynamically reconfigurable Embedded Computational Units (ECUs) memory, PLL’s and large amount of Programmable logic to give the user, ability to implement a wide range of real-time DSP applications.

- In normal PLD’s these DSP functions consume large amount of logic, which hampers the performance due to their interconnections.

- Software tools like DSP-wizard, QuickFilter are available from QuickLogic to use these devices.
QuickDSP Architecture.

- The modes of the ECU block are dynamically reprogrammable through instruction Set Sequencer.
- Instruction set sequencer is nothing but a FIFO loaded with either algorithms or state machines.

**FIGURE 2. ECU Embedded Computational Unit Block Diagram**

<table>
<thead>
<tr>
<th>Function</th>
<th>Description</th>
<th>Slowest speed grade</th>
<th>Fastest speed grade</th>
</tr>
</thead>
<tbody>
<tr>
<td>Adder</td>
<td>16 bit</td>
<td>8 ns</td>
<td>2.5 ns</td>
</tr>
<tr>
<td></td>
<td>32 bit</td>
<td>10 ns</td>
<td>5.6 ns</td>
</tr>
<tr>
<td></td>
<td>64 bit</td>
<td>12 ns</td>
<td>6.7 ns</td>
</tr>
<tr>
<td>Multiplier</td>
<td>8 x 8</td>
<td>10 ns</td>
<td>4.3 ns</td>
</tr>
<tr>
<td></td>
<td>16 x 16</td>
<td>12 ns</td>
<td>6.7 ns</td>
</tr>
</tbody>
</table>

**Performance of various devices.**

<table>
<thead>
<tr>
<th>Instruction Set</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0</td>
<td>Multiply</td>
</tr>
<tr>
<td>0 0 1</td>
<td>Multiply - Add</td>
</tr>
<tr>
<td>0 1 0</td>
<td>Accumulate</td>
</tr>
<tr>
<td>0 1 1</td>
<td>Add</td>
</tr>
<tr>
<td>1 0 0</td>
<td>Multiply (registered)*</td>
</tr>
<tr>
<td>1 0 1</td>
<td>Multiply - Add (registered)</td>
</tr>
<tr>
<td>1 1 0</td>
<td>Multiple - Accumulate</td>
</tr>
<tr>
<td>1 1 1</td>
<td>Add (registered)</td>
</tr>
</tbody>
</table>

CDAC, Nagpur

RAJ VARDHAN 9970917761
The QuickPCI family of devices includes the PCI bus controllers with high speed programmable logic.

- PCI modes available are Target only, Master / target or both with 32 / 64 bit at 33 / 66 / 75 MHz performance.
- QuickPCI family supports both 3.3V and 5V supply.

FIGURE 1. QL5030 Diagram
Quick RAM Architecture.

- This family embeds up to 82900 bits of high performance SRAM in an array of user configurable logic, enabling large RAM, ROM and FIFO functions to run at very high speed of 300MHz.
- This on-chip high speed memory interface enables a variety of applications, which were not possible to implement previously.

FIGURE 1. QuickRAM Block Diagram
Quick Logic Logic cell.

FIGURE 7. Efficiency and High Performance
MAX9000 architecture.

- Consists of three major parts
  - **Logic Array Blocks (LABs):**
    - Contains the basic logic blocks called as macrocells.
  - FastTrack Switch matrix.
    - Connects the internal LABs as well as I/Os.
  - Input Output block.
    - Interface to the external world.
Logic Array Blocks.

Fasttrack Interconnects
Logic Array Block - LAB

- Each LAB contains 16 macrocells, each having 5-Product terms.
- 16 macrocell outputs are connected to Row interconnects and 32 lines go to Column interconnects. (16 true and 16 complemented.)
- Thus the e input options for the product terms are 114.
  - 33 inputs from Fast-track interconnect, available in direct as well as complemented form.
  - 16 lines are local feed back lines, which also are available in direct as well as complemented form.
  - 16 lines from macrocells as shareable expander terms.
Figure 3. MAX 9000 Macrocell & Local Array

16 Local Feedbacks

16 Shareable Expander Product Terms

Parallel Expanders (from Other Macrocells)

Global Clear

Global Clocks

Macrocell Input Select

Register Bypass

Programmable Register

to Row or Column FastTrack Interconnect

Local Array Feedback

Alterra MAX

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Altera FLEX 10K devices.

- FLEX = Flexible Logic Element Matrix.
- Fabricated using SRAM based CMOS technology.
- Uses mixed grained approach for logic implementation.
- Utilizes LUT based architecture to implement combinational functionality.
- Interconnect structure is hierarchical and main interconnect structure is continuous leading to fast speed and predictable delay parameters before actual place and route.
Altera FLEX 10K devices.

- Contains two types of logic blocks, arranged in an array surrounded by a continuous interconnect structure.
- These Two types are called as :-
  - EAB (Embedded Array Block.)
    Contains larger memories to implement specialized functions in smaller area and with faster speeds.
  - LAB (Logic Array Block.)
    Contains general purpose configurable logic.
Altera FLEX 10K devices.

- Each row contains one EAB and rest LABs.
- These blocks communicate with each other and with the I/Os through the interconnect structure.
- Both types of blocks have local interconnects to optimize the performance.
- LAB contains 8 logic elements (LE), their associated carry chain, cascade chain and local interconnects.
- EABs are used to implement the mega functions like RAM, ROM, bigger functionalities in one level with small area usage and faster speeds.
- These blocks can be combined for bigger functionalities.
Logic element in the FLEX10k.

- Contains 4 input LUT to implement combinational functionality.
- Contains programmable flip-flop with synchronous enable and programmable clear and preset logic.
- Clock, preset and preset control signals on F/F can be driven by global signals, general purpose I/O pins or any internal logic.
- Programmable Flip-flop can be configured for D, T, JK or SR operations.
Logic element in the FLEX10k

- LE drives both local interconnect as well as Fast-track interconnect.
- Carry chain is associated with the LE to enable the fast arithmetic functions.
- Cascade chain is present in each LE to implement wide input functions, by combining the multiple LEs.
- F/F and LUT can be used independently for unrelated functionalities in the same LE.
- Global routing can also be used by internal signals.
Figure 4. Logic Element

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Features.

- Clock-Lock and clock-boost circuits are used to minimize clock skew and clock performance.
- Multi-Volt I/O capability with clamping diodes.
- Facility of open drain output.
- This series supports hot socketing.
- I/O element contains bi-directional facility with input and tri-state output buffer.
- User programmable pull-up, pull down, slew rate control are available with each and every I/O.
Actel Devices.

- Actel is the only manufacturer of the antifuse programmable logic devices.
- Actel act series belongs to Antifuse FPGA’s.
- The interconnection strategy is quite different for these devices.
- The logic block is more or less similar to other devices but the interconnection strategy is interesting for these devices.
Actel Devices.

- The basic logic blocks are called as “Logic modules”.
- These blocks are arranged in an array.
- Space between two rows of logic modules is called as channel.
- Two types of interconnects are available viz. Horizontal & vertical interconnects.
Actel Act interconnect resources.

- For any of the logic module total 8 inputs are available, 4 from upper channel and 4 from lower channel.
- These lines are called as “input stubs”.
- One output is available for each Logic module and is connected to one vertical line called as “output stub”.
- This output stub can communicate with 4 channels, two on upper side and two on lower side.
- Each column of the Logic modules have one vertical line called as LVT (long vertical line).
- Span is total height of the chip.
Actel Act interconnection strategy.

- At the crossing points of these vertical and horizontal lines one antifuse switch resides.
- By blowing the antifuse, a connection can be established.
- 25 horizontal lines run through the channel out of which 3 are for clock, Vdd and ground.
- The span of these lines is different, ranging from four Logic Modules to the entire width of the devices.