BiCMOS TECHNOLOGY

Submitted by:
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**ABSTRACT**

BiCMOS technology is a combination of Bipolar and CMOS technology. CMOS technology offers less power dissipation, smaller noise margins, and higher packing density. Bipolar technology, on the other hand, ensures high switching and I/O speed and good noise performance. It follows that BiCMOS technology accomplishes both - improved speed over CMOS and lower power dissipation than bipolar technology. The main drawback of BiCMOS technology is the higher costs due to the added process complexity. Impurity profiles have to be optimized to both NPN and CMOS issues. This greater process complexity results in a $1.25\ldots1.4$ cost increase compared to conventional CMOS technology. The primary approach to realize high performance BiCMOS devices is the addition of bipolar process steps to a baseline CMOS process. We discuss in this section a $0.8\mu m$ BiCMOS process flow, emphasizing reliability, process simplicity and compatibility with a $0.8\mu m$ CMOS technology. Its wide application is in integration of semicustom & full custom ICs, standard cells, Gate arrays.
INTRODUCTION

Integration, speed and power improvements achieved using silicongermanium bipolar transistors have enabled new types of functionality in high-performance integrated circuits. After a discussion of some applications that benefit from the use of SiGe BiCMOS technology, this paper describes a production process with bipolar $F_t$ of 150 GHz and $F_{max}$ of 170 GHz. The modularity of this technology enables cost and performance trade-offs that make it suitable for different market segments. Leveraging the same manufacturing infrastructure and tools that are used for mainstream CMOS technology makes it possible to provide the predictable performance and high yield that is expected in silicon manufacturing. SiGe BiCMOS technology addresses a number of different market segments. A state-of-the-art example provides a variety of features while maintaining the benefits of manufacturing silicon-based technology. The primary approach to realize high performance BiCMOS devices is the addition of bipolar process steps to a baseline CMOS process. We discuss in this section a $0.8\mu m$ BiCMOS process flow, emphasizing reliability, process simplicity and compatibility with a $0.8\mu m$ CMOS technology.
MANUFACTURABILITY

A key to manufacturability of SiGe technology is the reuse of high-volume CMOS infrastructure. The maturity of process equipment, the high level of factory automation for recipe download and wafer handling, the yield management discipline and the mechanisms for continuous improvement make it possible to high quality wafers in complex process technologies. For similar process complexity, as measured by the number of critical photomask layers or the number of process steps, the manufacturing cost and fab yield is comparable regardless of the technology specifics. It is the commitment to establishing process modules that are within the capability of the equipment set that makes it possible to deliver SiGe technology that is as repeatable and cost effective as mainstream CMOS. The ability to perform in-line measurement of SiGe epi thickness, germanium content and boron doping level is required to establish typical production control charts. Spectroscopic ellipsometry can be used on production wafers to monitor SiGe epi thickness. Demonstrated control of 1.64% 1-sigma variation provides feedback on the epi process. Measurement of poly thickness and in-line sheet resistance closes the loop for day-to-day SiGe manufacturing.

BiCMOS Process Technology

BiCMOS technology is a combination of Bipolar and CMOS technology. CMOS technology offers less power dissipation, smaller noise margins, and higher packing density. Bipolar technology, on the other hand, ensures high switching and I/O speed and good noise performance. It follows that BiCMOS technology accomplishes both - improved speed over CMOS and lower power dissipation than bipolar technology. The main drawback of BiCMOS technology is the higher costs due to the added process complexity. Impurity profiles have to be optimized to both NPN and CMOS issues. This greater process complexity results in a 1.25…1.4 cost increase compared to conventional CMOS technology.
The primary approach to realize high performance BiCMOS devices is the addition of bipolar process steps to a baseline CMOS process. We discuss in this section a BiCMOS process flow, emphasizing reliability, process simplicity and compatibility with a CMOS technology.

The integration of the bipolar process steps into the baseline CMOS process flow is given by Table 1. First, the P+ substrate is replaced by a P- substrate material to incorporate the NPN device into the N-well of the PMOS device. This lower doped substrate increases the susceptibility for latchup. To improve latchup immunity retrograde N-well doping is used. The retrograde doping can be either achieved by

<table>
<thead>
<tr>
<th>CMOS</th>
<th>Changes for Bipolar</th>
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<tr>
<td>P+ Substrate</td>
<td>P- Substrate</td>
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<td></td>
<td>Buried N+/P-Layer</td>
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<tr>
<td>P- EPI</td>
<td>intrinsic doped EPI-Layer</td>
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<td>N-Well / P-Well</td>
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<td>Well drive-in</td>
<td>reduced drive time</td>
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<td>Poly Buffer Locos</td>
<td>high pressure Oxidation</td>
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<td></td>
<td>Deep Collector/N+ Resistor</td>
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<td></td>
<td>Base/P Resistor</td>
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<td>(V_t) Implant</td>
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<tr>
<td>Gate Oxidation (200 Å)</td>
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<tr>
<td>Poly Deposition/Doping</td>
<td>Poly Deposition</td>
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<td>Emitter Pattern/Etch</td>
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<td></td>
<td>Implant Poly Emitter</td>
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<tr>
<td>Pattern/Etch Poly</td>
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<tr>
<td>LDD Pattern/Implant</td>
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<tr>
<td>SWO Deposition/Etch</td>
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<tr>
<td>Pattern/Implant N+/P+ S/D</td>
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<tr>
<td>Anneal S/D</td>
<td>Anneal optimized for Emitter</td>
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Table 1: BiCMOS process flow showing the integration of a bipolar process into an existing baseline CMOS process
high energy ion implantation or by using buried layers. With the first approach no epitaxial layer is required, but ion implantation damage has to be considered.

By using buried layers a relatively thick and expensive epitaxial layer has to be grown on top of the substrate. This epitaxial layer hosts the collector of the NPN as well as the P-well and the N-well of the CMOS devices. The epitaxial deposition process must be optimized to reduce material defects and minimize autodoping. Due to the usage of the buried layers the well drive-in has to be optimized for bipolar collector requirements. From the bipolar point of view the collector profile should consist of a thin heavily doped collector region (buried N+ layer) and a thick lightly doped collector region on top. The first one minimizes the Kirk effect, where the second one ensures higher collector-base breakdown voltage. The CMOS device on the other hand requires a sufficiently high concentration below the surface to avoid punchtrough, especially as device dimensions are shrinking. Practically,
the various conflicting requirements have to be balanced.

This leads to steeper collector N-well profiles which cause an increase of the collector series resistance. To improve the collector series resistance a deep subcollector N+ diffusion is used.

Finally, the same polysilicon material is used for the fabrication of the NMOS and PMOS gates as well as for the bipolar polysilicon emitter. The doping for the emitter junction is usually provided by a N-type implant into the polysilicon, which forms the emitter-base contact during the source-drain anneal of the CMOS device by outdiffusion. The N-type polysilicon gates result in a surface channel NMOS device and a buried channel PMOS device.

We start up with a lightly-doped P-type wafer and form the buried N+ layer by ion implantation of antimony into the respective mask pattern. The pattern is etched in a 50nm thick oxide covering the substrate. The structure before the antimony implantation is shown in Figure 1. Afterwards, a high temperature anneal is performed to remove damage defects and to diffuse the antimony into
the substrate. During this anneal an oxide is grown in the buried N+ windows to provide a silicon step for alignment of subsequent levels. To achieve breakdown between the buried N+ regions a self-aligned punchthrough implant is performed. Therefore, the nitride mask is selectively removed and the remaining oxide serves as blocking mask for the buried P-layer implant (see Fig. 2).

**Figure 1:** Device cross-section of BiCMOS process showing N+ buried layer implant.

After removing all oxide a 1.5\(\mu\text{m}\) thick epitaxial layer with intrinsic doping is grown on top (see Fig. 3). After the buried layer alignment is finished, a twin well process is used to fabricate the N-well of the PMOS and the collector of the NPN device. Therefore, the same masks are used as for the buried layers. Again, the wafer is capped with a nitride layer which is opened at the N+ regions. After implanting the N-type dopant a 350nm thick oxide is grown and the nitride is stripped from the P+
regions. The subsequent P-well implant is self-aligned to the well edge (see Fig. 5). As compared to conventional CMOS a relatively short well drive-in (200 min) is performed at 1000°C with the oxide cap in place.

**Figure 3:** Device cross-section of BiCMOS process after growth of the EPI-layer.

**Figure 4:** Device cross-section of BiCMOS process showing EPI-layer masking for N-well implant.

**Figure 5:** Device cross-section of BiCMOS process showing self-aligned P-well implant. Previously, the N-wells were implanted and a 350nm oxide is grown, which serves as blocking mask for the P-well implant.
After the wells are fabricated the whole wafer is planarized and a pad oxide is grown. The oxide is capped with a thick nitride. After patterning the active regions of the device, an etch step is used to open up the field isolation regions. Prior to field oxidation, a blanket channel stop is implanted (see Fig. 6).

**Figure 6:** Device cross-section of BiCMOS process showing channel stop implant. Before, the wafer was planarized and patterned.

Oxidation is used to fabricate a 850nm thick field oxide. To minimize buried layer diffusion the oxidation temperature is quite moderate (975°C). After removal of the nitride masks from the active regions the structure is patterned to implant the deep N+ subcollector. Therefore, phosphorus is implanted into the N-well of the collector region (see Fig. 7).
The PMOS and NMOS devices are protected by the photoresist. We continue with the fabrication of the intrinsic base for the bipolar device. Therefore, the base region is opened and the base implant is performed. To ensure low base-emitter capacitance a thicker gate oxide is deposited after the base implant. This oxide will also serve as implantation shelter for the base region caused from the CMOS threshold implants. The deposited oxide has to be removed from the non base regions by an etch step. The structure after the intrinsic base implant and prior to the base oxide deposition is shown in Figure 8.
The emitter window is opened, followed by the polysilicon deposition. The polysilicon is implanted and will serve as outdiffusion source to form the emitter junction. We proceed with the resist strip and perform a pre-gate oxide etch to clean the oxide surface. A 20\text{nm} thick gate oxide is grown on top. The active emitter window is patterned and opened up with an etching process until the whole gate oxide is removed in the emitter region. Then a polysilicon layer is deposited, which forms the emitter contact as well as the gate polysilicon layers. This polysilicon layer is implanted with arsenic which will diffuse out from the polysilicon layer at the final source-drain anneal to form the emitter junction (see Fig. 9).
Figure 10: Device cross-section of BiCMOS process before the NMOS LDD doping is implanted. The subcollector is opened to collect additional N-type doping.

Figure 11: Device cross-section of BiCMOS process showing the source-drain implantation of the NMOS device. Again, phosphorus is implanted into the subcollector region.

The polysilicon layer is patterned to define the CMOS gates and the bipolar emitter. After emitter formation, all subsequent process steps are well known from CMOS technology. Phosphorus is implanted to form a shallow LDD region for the NMOS device (see Fig 10). Then the sidewall spacer formation is initiated. Therefore, an oxide layer is deposited and anisotropically etched back. Next, the source-drain regions are heavily doped by phosphorus and boron, which is depicted in
Figure 11 and Figure 12, respectively. The P+ source-drain implant is also used for the extrinsic base fabrication.

Finally, the fabrication of the active regions is finished by the source-drain anneal, which is optimized for outdiffusion conditions of the bipolar device. Hence, a 15s long RTA anneal at 1050°C is performed. The final device structure including the active area dopings is shown in Figure 13.

**Figure 12:** Device cross-section of BiCMOS process showing the PMOS source-drain implantation, which is also applied to the base to form the extrinsic base doping.

**Figure 13:** Device cross-section of BiCMOS process after fabrication of the active areas.
The source-drain anneal is optimized to emitter outdiffusion conditions. Afterwards the structure is scheduled for a double-level interconnect process.

**HIGH-PERFORMANCE TECHNOLOGY**

Multiple generations of BiCMOS technology demonstrate rapid advances in bipolar performance. A production 0.18 m SiGe BiCMOS technology (SiGe120) with $F_t=150$ GHz and $F_{max}=170$ GHz begins with collector formation using a buried layer and substrate epi. Utilizing both shallow and deep trench isolation, a self-aligned SiGe NPN is formed after most of the standard dual-gate 0.18 m CMOS steps. Blanket SiGe epitaxy is performed in a single-wafer RT-CVD. A sacrificial emitter post is patterned using DUV lithography to achieve scaling comparable to CMOS gates. Self-aligned extrinsic base implants enable optimization of extrinsic base resistance while maintaining a simple bipolar structure. After removal of the sacrificial emitter and pre-clean steps, an in-situ doped poly emitter is deposited in an RT-CVD reactor and patterned. The subsequent cobalt silicide formation, contact etches and oxides CMP are the same as the standard CMOS process. The SiGe120 process continues with 4 layers of standard metallization, thin film metal resistor, and MIM capacitor plus 2 thick layers of aluminum (1.5 m and 3.0 m) for implementation of transmission lines and inductors.

**APPLICATIONS FOR BICMOS**

SiGe bipolar transistors can now match or exceed the performance of production III-V technologies. Mainstream acceptance has made SiGe BiCMOS cost competitive with advanced CMOS. Increased RF sub-system functionality is driving new architectures, like direct conversion radios, which reduce the dependence on off-chip components while the requirements of next generation products are more demanding in terms of noise figure, gain, linearity and power consumption than the current generation. Physical layer products for 10G and 40G systems have migrated to more highly integrated SiGe BiCMOS designs that have increased functionality, reduced power and reduced cost. Increased data...
density in disk drives is leading to a need for higher data rate and greater sensitivity pre-amplifiers that require SiGe BiCMOS. Developing standards, such as Ultra-Wide-Band for wireless data, can exploit the performance offered by SiGe BiCMOS to meet the 2-11 GHz frequency requirements while meeting power and cost targets consistent with a consumer application. Its typical applications are-

- Full custom ICs
  - SRAM, DRAM
  - Microprocessor, controller
- Semi custom ICs
  - Register, Flipflop
- Standard cells
  - Adders, mixers, ADC, DAC
- Gate arrays

**ADVANTAGES**
- Improved speed over CMOS
- Improved current drive over CMOS
- Improved packing density over bipolar
- Lower power consumption than bipolar
- High input impedance
- Low output impedance

**DISADVANTAGES**
- Increased manufacturing process complexity
- Speed degradation due to scaling

**COMPARISON between BASIC CMOS & BiCMOS**
- SPEED COMPARISON

- DELAY COMPARISON

- AREA COMPARISON
CURRENT STATUS AND FUTURE TRENDS

- SiGe BiCMOS HP
- SiGe BiCMOS WL
- SiGe HBT

BiCMOS PRODUCTS

SiGe BiCMOS GPS CIRCUIT  GSM 900 POWER AMPLIFIER

W-CDMA DCR
CONCLUSION

- The extra process complexity requires chip manufacturers to command a premium for BiCMOS products. In the analog market the ability to integrate large mixed systems provides the compelling cost advantage of BiCMOS; this market is still emerging.
- BiCMOS is a complement to pure CMOS and Bipolar technologies in important system application areas.
- SiGe BiCMOS technology addresses a number of different market segments. A state-of-the-art example provides a variety of features while maintaining the benefits of manufacturing silicon-based technology.

REFERENCES