A Feedback Controlled Impedance Matching System for Ultrasonic Transducers

by

Elliot Briggs, BSEE

A Thesis

In

ELECTRICAL ENGINEERING

Submitted to the Graduate Faculty
of Texas Tech University in
Partial Fulfillment of
the Requirements for
the Degree of

MASTER OF SCIENCE

IN

ELECTRICAL ENGINEERING

Approved

Dr. Brian Nutter, Ph.D. PE
Committee Chair

Dr. Dominick Casadonte, Ph.D.
Committee Co-Chair

Dr. Mohammad Saed, Ph.D.

Fred Hartmeister
Dean of the Graduate School

December, 2009

Acknowledgements

I would like to express my most sincere gratitude to Dr. Nutter and Dr. Casadonte for their expert advice and support throughout this project. A great deal of thanks is also owed to Dr. Saed for his willingness to serve on my thesis committee.

The financial support of the Department of Chemistry and Biochemistry as well as the Department of Electrical Engineering is acknowledged and greatly appreciated.

I would like to especially thank my wife for her continuous patience and support throughout the time spent on this project. Without the support of my wife, parents, family, and the excellent faculty of the Texas Tech Electrical Engineering Department, this project would not have been possible.

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Abstract

In order to deliver maximum power into a reactive load using a 50 Ω source, one must transform the load impedance to 50 Ω. This thesis will discuss a particular application that has been provided by the Texas Tech Department of Chemistry & Biochemistry that requires maximum power to be delivered into a piezoelectric transducer that possesses a resistive, reactive and variable load impedance. For this application, a device must be created that will not only provide an impedance match to maximize power transfer into the transducer, but will do so continuously, autonomously and reliably.

Chapter 1

Introduction

Researchers in the Department of Chemistry and Biochemistry have been performing research in an field called "Sonochemistry". This field involves the study of the effects that high-frequency acoustic waves have on chemical reactions. To create the acoustic waves, a device converts electrical energy into mechanical energy using the piezoelectric effect. A device that converts one type of energy, electrical, into another type of energy, mechanical, is often referred to as a "transducer". The transducer is made of a special ceramic that expands and contracts when an electric potential is applied. By applying an alternating current, the device will rapidly expand and contract at the frequency of the electrical signal. The rapidly expanding and contracting transducer creates an acoustic wave that will travel through the medium in which the chemical reaction takes place.

The transducer is made of a certain piezoelectric material, lead zirconate titanate, also known as PZT, and is constructed in a specific geometry. These parameters greatly determine the transducer's frequency response and electrical characteristics. Because a specific transducer has already been chosen for this application, the relation of the transducer's electrical properties with frequency and temperature is of interest. As an electrical signal is applied to the transducer, heating can occur as power is dissipated. As the transducer warms, the transducer's electrical characteristics will change. Because the transducer is a resonant device, a slight change in frequency can also affect the electrical properties. The combined effects of changing temperature and frequency cause the delivered acoustic power to the chemical reaction to be variant. In this application, a constant and maximum level of acoustic power is desirable.

A device must be made that continuously measures the electrical properties of the transducer and can compensate for any variations. By continuously measuring and compensating for the varying electrical properties of the transducer, acoustic power can be made maximum and constant. It is also advantageous for the device to make the

necessary compensations with minimal human interaction. The design of such a device is the topic of this thesis.

1.1 Previous Work

Work has been done in the past to maximize the electrical power transfer into piezoelectric transducers. The resistive and capacitive impedance of the transducer over the frequency range of interest was exploited and a device was made to maximize power transfer into a load of this nature. The created device however does not take measurements or offer any feedback to the user to influence any adjustment decisions. Because the transducer has a varying impedance with frequency and temperature, any adjustments made without accurate measurements are likely to yield less than maximum power transfer, especially as these parameters change over time. Also, the device that was previously constructed is very large and cannot easily be transferred between labs or be used in a field testing environment without considerable effort. It is of great interest to improve portability and user friendliness.

All of the aforementioned problems will be addressed in the design of a new system. In the new design, the user will have minimal interaction in the impedance matching process, the system will be capable of providing measurement data to the user, and the system will be more practically sized than previous designs to ease transportation effort.

Chapter 2

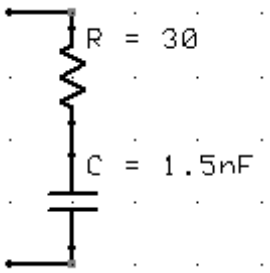
Impedance Measurement

A large portion of the discussion regarding the system's design considerations will be devoted to effective impedance measurement and understanding how to derive a control signal that will allow automatic operation. In order to understand how impedance can be measured, some background must be introduced.

2.1 Mathematic Background for Impedance Measurement

The system being designed must be able to match the source and load impedances. The signal source in this application is a laboratory signal generator and the load is a piezoelectric transducer. The signal generator's impedance can be described using a complex number, $50 + j0\ \Omega$. When describing impedance, the complex notation will often be used because impedance is complex, even though the imaginary part may be zero. The real part of the complex number represents the impedance's real resistance and the imaginary part represents the reactance. For example, the signal generator has a resistance of $50\ \Omega$ and a reactance of $j0\ \Omega$**.** By definition, a passive device such as the transducer can only dissipate power; therefore the reactance is allowed to be negative, but the resistance is not. If a resistance is negative, current is generated by the element rather than resisted. An arbitrary negative reactance $-jX$ means that the imaginary part, or reactance of the described impedance is capacitive. A positive reactance $+jX$ means that the impedance is inductive. Example conversions of an RC and RL network into complex impedance notation are shown below.

In this example, a real 30 Ω resistance and capacitance must to be converted to a reactance. The frequency will be set to 500 kHz.



$$impedance = R + \frac{1}{j\omega C}$$

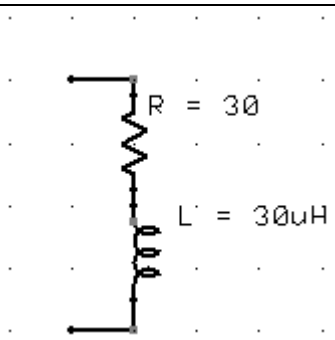
$$= 30 + \frac{1}{j(2\pi)(500 \times 10^3)(1.5 \times 10^{-9})}$$

$$= 30 - j212.2\ \Omega$$

Figure 1: RC network

The resulting impedance is $30 - j212.2\ \Omega$. Note that a property of imaginary numbers allows the numerator and denominator to multiplied by the conjugate of the denominator, eliminating the j in the denominator and bringing it to the numerator as $-j$. This results from the fact that $j \times -j = 1$. The preferred notation has no imaginary numbers in the denominator.

A similar example will be carried out on an RL network. 500 kHz again will be used for the frequency.



$$impedance = R + j\omega L$$

$$= 30 + j(2\pi)(500 \times 10^3)(30 \times 10^{-6})$$

$$= 30 + j94.25\ \Omega$$

Figure 2: RL network

The resulting impedance is $30 + j94.25\ \Omega$. In this example, the imaginary term is not in the denominator, making the reactance positive.

Now that representation of impedances as complex numbers has been illustrated, these numbers can be mapped in the complex plane, where the real and imaginary parts both represent axes in a Cartesian coordinate system.

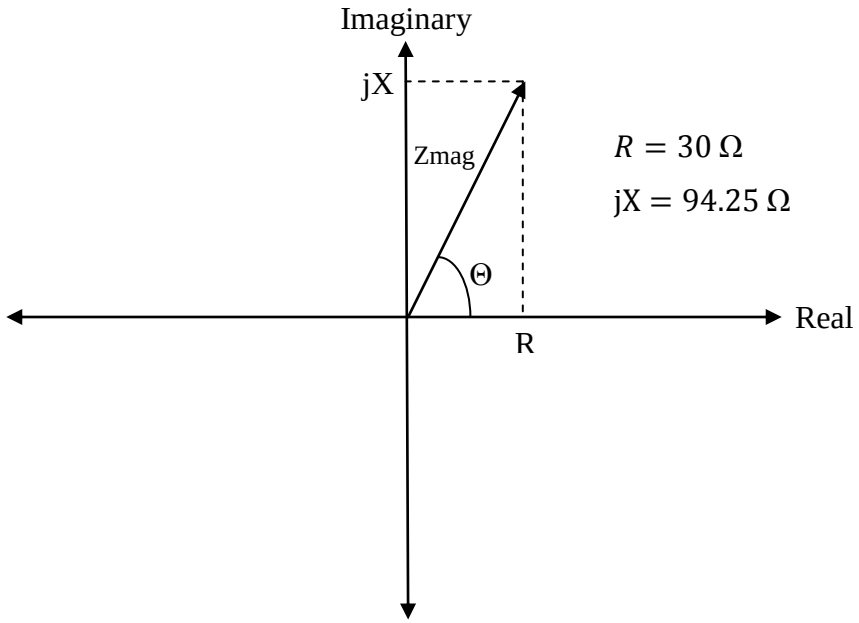


Figure 3: Impedance in the Complex Plane

Taking the RL network of Figure 2 and assigning the real part of the impedance to the real axis and the imaginary part to the imaginary axis, the vector will appear as in Figure 3. Both the real and the imaginary parts are positive ($30 + j94.25\ \Omega$), and therefore the vector will originate at the origin and extend out into the first quadrant as the coordinates of the real and imaginary part dictate. The magnitude and phase of this vector become quite important in impedance measurement. Measuring both of these parameters can lead to the determination of the measured circuit's impedance. In order to find the magnitude of the vector, Pythagoras' theorem says the length of the hypotenuse (c) of a right triangle can be found if the two legs of the triangle (a and b) are known.

$$c = \sqrt{a^2 + b^2}$$

The values of a and b are known, which are the real and the imaginary part of the RL circuit impedance. The imaginary and real parts of the RL circuit's impedance are inserted into the above equation as the two legs of the triangle. The result will be called

Z_{mag} because it will be the magnitude of the impedance, complex impedance is often referred to as Z.

$$Z_{mag} = \sqrt{30^2 + 94.25^2} = 98.9\ \Omega$$

Now that the magnitude of the impedance is known, the angle of the vector relative to the real axis, θ, must be found.

$$tan(\theta) = \frac{\Im\mathfrak{m}\{impedance\}}{\Re\mathfrak{e}\{impedance\}}$$

$$\theta = tan^{-1}\left(\frac{\Im\mathfrak{m}\{impedance\}}{\Re\mathfrak{e}\{impedance\}}\right)$$

$$\theta = tan^{-1}\left(\frac{94.25}{30}\right) = 72.34°$$

These two values can be taken to represent the impedance in phasor notation.

$$Z_{mag} \angle\theta$$

Using phasor notation, the impedance of the RL circuit is representation is shown below.

$$98.9\angle 72.34° \ \Omega$$

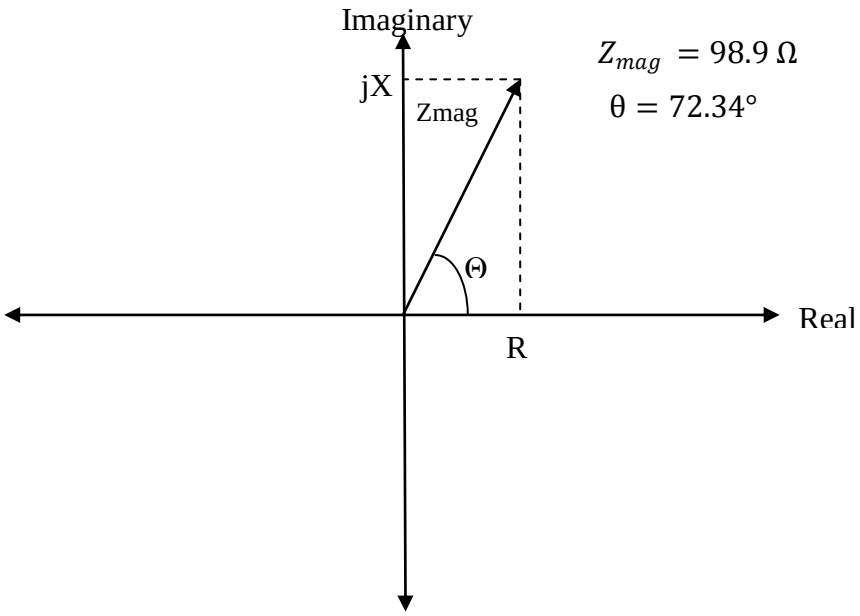


Figure 4: Complex Impedance (Phasor Notation)

Upon inspection of the above figure, returning to Cartesian coordinates is a simple task involving trigonometry. If the angle θ and the impedance magnitude Z_{mag} are known, the rectangular impedance coordinates can be found using the equation below.

$$R + jX = Resistance + jReactance$$

$$= cos(\theta) \times Z_{mag} + j\big(sin(\theta) \times Z_{mag}\big)$$

This impedance can easily be transformed back to the original inductance value given the frequency. For an inductive impedance,

$$jX = j\omega L = j2\pi f L$$

$$L = \frac{jX}{j2\pi f} = \frac{X}{2\pi f} = \frac{sin(\theta) \times Z_{mag}}{2\pi f} = \frac{sin(72.34°) \times 98.9}{2\pi(500 \times 10^3)}$$

$$= 30 \times 10^{-6}\ \text{H} = 30\ \mu\text{H}$$

To extract a capacitance from phasor notation a similar method is used.

$$jX = \frac{1}{j\omega C} = \frac{1}{j2\pi fC}$$

$$C = \frac{1}{j2\pi fjX} = -\left(\frac{1}{2\pi fX}\right) = -\left(\frac{1}{2\pi f\left(sin(\theta) \times Z_{mag}\right)}\right)$$

Because the reactance X in a capacitive load by definition is always negative, C will be positive as expected. For consistency, the same exercise will be carried out with the RC load shown in figure 1. Recall,

$$Z = 30 - j212.2\ \Omega$$

$$\theta = tan^{-1}\left(\frac{-212.2}{30}\right) = -81.95°$$

$$Z_{mag} = \sqrt{30^2 + (-212.2)^2} = 214.31\ \Omega$$

$$C = -\left(\frac{1}{2\pi(500 \times 10^3)(sin(-81.95°) \times 214.31)}\right)$$

$$= 1.5 \times 10^{-9}\ \text{F} = 1.5\ \text{nF}$$

This method will be the basis of how impedance will be measured. The next step is to understand how the θ and Z_{mag} values are obtained.

2.2 Measurement Methods

It has been shown that if θ and Z_{mag} are obtained, impedance and even inductance and capacitance can be derived if the frequency is known. In this section, methods of measuring these parameters will be discussed.

2.2.1 Measuring Impedance Magnitude

Impedance magnitude Z_{mag} to this point has been written with the unit Ohms (Ω). This is indicative of how Z_{mag} is obtained. Ohm's law states

$$R = \frac{V}{I}$$

In a circuit that contains both resistive and reactive elements, the current is shifted in phase by the angle θ relative to the voltage. As an example, Ohm's law will be applied to the inductive load that was defined in **Error! Reference source not found.**. For analysis, a voltage source of $1\angle 0°$ will be applied to the load as shown in Figure 5.

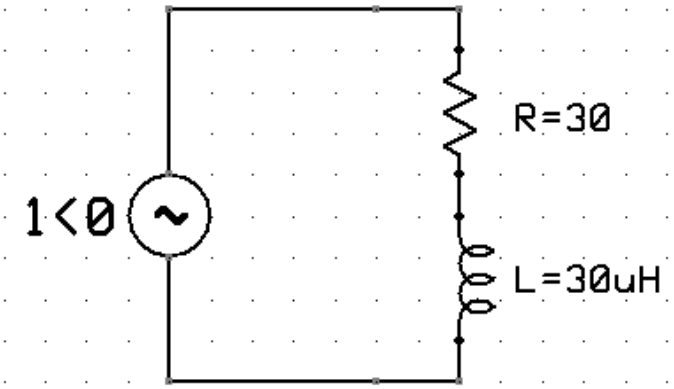


Figure 5: RL Test Load with Source

Ohm's law is applied below to find the current in the circuit. Note that R has been replaced with Z.

$$I = \frac{V}{Z} = \frac{1\angle 0°}{98.9\angle 72.34°} = 10.1112 \times 10^{-3}\angle -72.34° \text{ A}$$

The angle of the current indicates that it is lagging behind the voltage by $-72.34°$, which will be verified and discussed in the 2.2.2 Measuring Phase section. If the angles of the voltage and current are not considered and only the magnitudes are used, the vectors become scalar. When only the vector magnitudes are considered, Ohm's law can be used to find the ratio of voltage and current amplitude, which is Z_{mag} .

$$\|I\| = \frac{\|V\|}{\|Z\|} = \frac{1}{98.9} = 10.1112 \times 10^{-3} \text{ A}$$

$$Z_{mag} = \|Z\| = \frac{\|V\|}{\|I\|} = \frac{1}{10.1112 \times 10^{-3}} = 98.9\ \Omega$$

This reveals the ability to measure the magnitude of the voltage and current and directly calculate the impedance magnitude Z_{mag}.

To measure the magnitude of the current and voltage, a peak detector can be used to measure the positive peaks of the sinusoid's crest. Many peak detecting circuit designs have been developed, almost all of which consist of a rectifier and a low-pass filter.

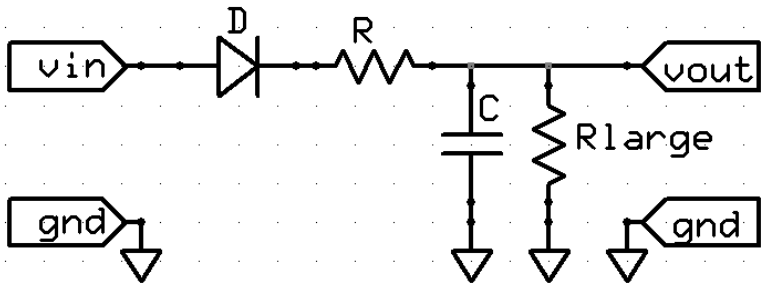


Figure 6: Single Diode Peak Detector

The above circuit shows a simple rectifier and filter that perform peak detection. When the voltage at Vin exceeds the forward voltage of the diode, the diode conducts and charges the capacitor through the resistor R. The resistor Rlarge is chosen so that the ratio between Rlarge and R is very large, making the voltage divide between the two resistors negligible. The charge rate of the capacitor is limited by the size of the capacitor C and resistor R that is used. The 3 dB cutoff frequency of this filter is approximated below. Assume the diode has zero resistance when forward biased and Rlarge is approximated as an infinite resistance.

$$f_{3dB} = \frac{1}{2\pi RC}$$

If f_{3dB} is much lower than the frequency present in the signal at Vin, the filter will quickly reach and "hold" the maximum value seen at Vin, effectively "peak detecting". After the capacitor is charged to the peak voltage, Rlarge will slowly drain charge out of the capacitor at a very slow rate. This allows the circuit to gradually reset itself over time

if no additional peaks are large enough to make the diode conduct. After some time, Rlarge drains enough charge from C to allow smaller peaks to cause the diode to conduct. If Rlarge was not present, the capacitor would simply become charged by the highest peak Vin voltage and would hold that charge forever (assuming no charge in the capacitor escapes through parasitic elements). In application, a high input impedance measurement circuit such as a buffer amplifier will draw very small amounts of current from the capacitor. If the input resistance of the measurement circuit is on the order of Rlarge, Rlarge can be eliminated.

Some drawbacks to this design may be obvious. Whenever the diode conducts, current is drawn very suddenly from the signal being measured. This is not always acceptable. A buffer amplifier may have to be added so that the circuit is isolated from the signal being measured. Another disadvantage to this design is the diode typically will induce a .3 - .7 V drop on the signal present at Vin. This makes the voltage stored on the capacitor not equal to the actual peak voltage seen at Vin, but reduced by the diode's forward voltage, which is unattractive in measurement applications. The actual forward voltage drop of the diode is not constant. The forward voltage of the diode varies with device, temperature, and current. The design in Figure 6 also may exhibit an intolerably high amount of ripple at Vout. In this design, ripple is caused by the diode only conducting on the positive portion of the waveform at Vin, allowing the capacitor to drain some of its charge through R during the negative portion. Ripple at Vout will be high if the capacitor is able to quickly drain a significant portion of its charge during this time. Ripple levels can be decreased by reducing the cutoff frequency of the low-pass filter section at the expense of reduced response time to large peaks.

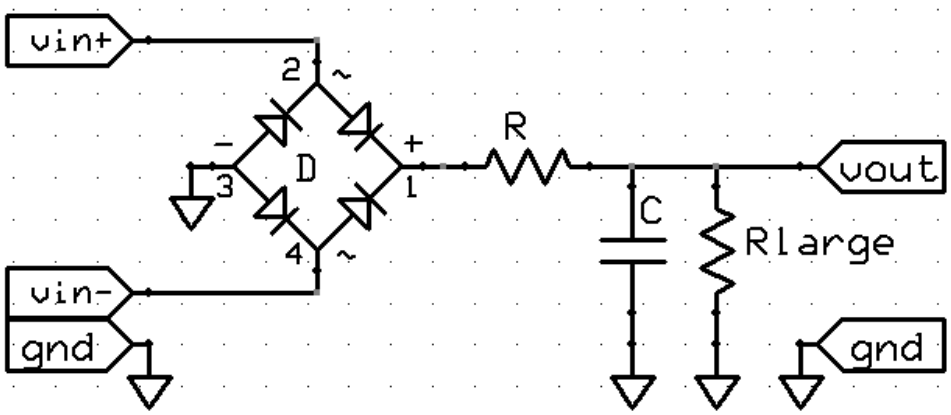


Figure 7: Diode Bridge Peak Detector

The above circuit is a variant of the circuit displayed in Figure 6. The single diode has been replaced with a diode bridge, an arrangement of four diodes that acts as a full-wave rectifier instead of the previous half-wave design. This diode arrangement helps the ripple problem that the previous circuit possessed, but it exacerbates the diode voltage drop problem. Instead of the single diode conducting on the positive portion of the measured waveform, the diode bridge has two diodes that each conduct on the positive or negative portion of the waveform. The current from Vin passes through two diodes, making the diode voltage drop double that of the single diode circuit given that the diodes in the circuits are identical. A problem that has not yet been mentioned in either circuit is DC offset tolerance. Both of the described peak detectors are vulnerable to DC offset and both respond differently. The single diode circuit is only a half-wave rectifier, so a DC offset in Vin will only produce a DC offset in Vout. The peaks of the sine are simply shifted according to the DC offset. The full-wave rectifier will introduce large amounts of ripple depending on the level of DC offset. In the full-wave rectifier, both the positive and negative portion of the waveform are being passed into the filter. Therefore, if a DC offset is present, the positive and negative portions of the wave will be asymmetrical and may produce excessive ripple at the output of the circuit. Both of these peak detecting circuits have less than desirable drawbacks when used in a measurement application. The biggest problem from a measurement standpoint is the unreliable or unpredictable diode forward voltage drop. A circuit exists with very desirable features that overcome this

problem. Such a circuit is commonly referred to as a "precision rectifier". These circuits typically use opamps as well as diodes to rectify without a diode voltage drop. First, the rectifier section is introduced.

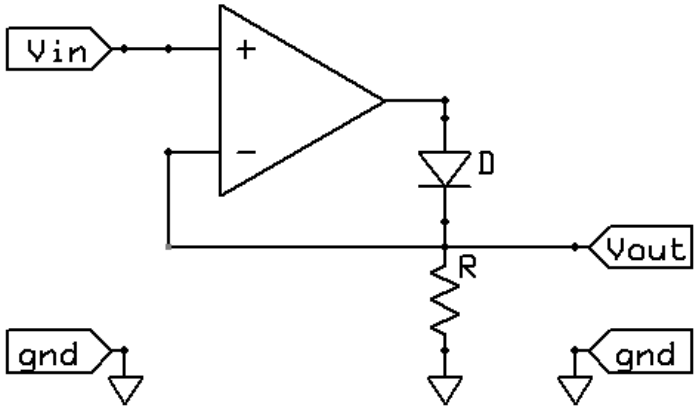


Figure 8: "Precision" Rectifier

In the circuit displayed in Figure 8, a negative voltage present at Vin will cause the voltage at the output pin of the opamp to be negative, causing the diode to not conduct current. When the diode is not conductive, no current will flow into the resistor R and no voltage will be present at Vout. When a positive voltage is present at Vin, the output of the opamp will produce a positive voltage. This causes the diode to slightly conduct as the voltage at the output reaches the diode's forward voltage and becomes fully conducting. In the meantime, the opamp senses the voltage on the node shared by the diode and the resistor because this voltage is fed back into the opamp's inverting input. The opamp, based on the voltage sensed on the inverting input, will adjust its output so that the voltage seen between the diode and resistor is equal to Vin. This effectively eliminates the forward voltage drop problem that previously mentioned circuits possess. This circuit also greatly isolates Vin and Vout. When the diode conducts, current will be drawn from the pin of the opamp instead of from the signal waveform itself, which is highly desirable in a measurement application.

The resulting output from a sinusoidal input will be the input waveform with the negative portion clipped at zero and negligible diode forward voltage effects. The output

waveform's peak will be the same as the peak at the input. To convert this circuit into a peak detector, a low-pass filter will smooth the waveform seen at Vout into a quasi DC level. Figure 9 displays the "precision" peak detector.

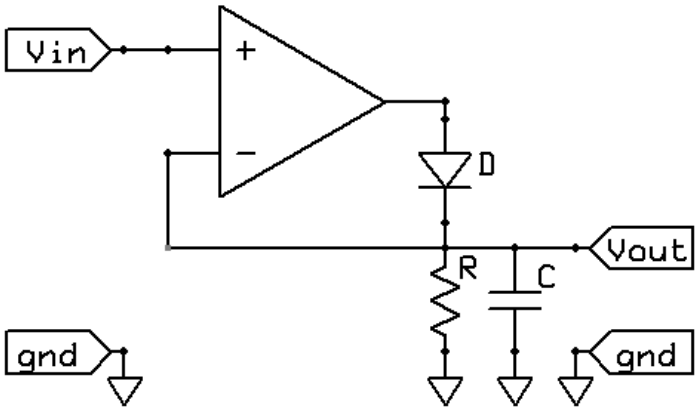


Figure 9: "Precision" Peak Detector

The only difference between the peak detector and the rectifier circuit is the capacitor placed between Vout and ground. When a positive voltage is present at Vin, the output pin will be positive and will cause the diode to slightly conduct as it approaches the diode's forward voltage at which the diode will fully conduct. When the diode conducts, it quickly charges the capacitor to the voltage present at Vin. The only current path in which charge can to drain from the capacitor is through the resistor Rlarge, which is added to slowly drain the capacitor's charge so that the circuit can detect other peaks after a large peak has caused the capacitor to be charged to a relatively high voltage. This circuit will detect the voltage magnitude V_{mag} that is of interest in calculating Z_{mag}.

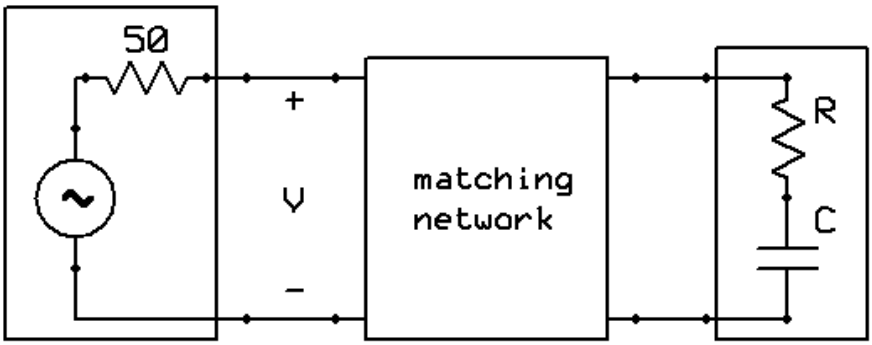


Figure 10: Vmag Measurement Point

Figure 10 indicates where the Vmag measurement is taken; before the matching network and load. If a feedback control system is going to servo the matching network to deliver maximum power transfer into the load, the ratio of voltage and current amplitudes supplied by the source must be 50/1, or 50 Ω. By measuring the voltage and current at the output of the source, the ratio can be used as a control signal.

Calculating the current magnitude I_{mag} will require a circuit to convert current into a voltage that can be "peak detected". It is very common in current measurement applications to include a very small sense resistor in series with the current to be measured. The voltage measured across a resistor indicates the current flowing through it if the resistance is known. The example below shows that if 1 V is measured across a 1 Ω resistor, the current flowing through the resistor must be 1 A.

$$I = \frac{V}{R} = \frac{1}{1} = 1 \text{ A}$$

The same concept in the equation above is used in the circuit displayed in Figure . A differential amplifier has been added that measures the voltage across a small resistor Rsense (gain setting resistors used in the differential amplifier have been omitted for clarity).

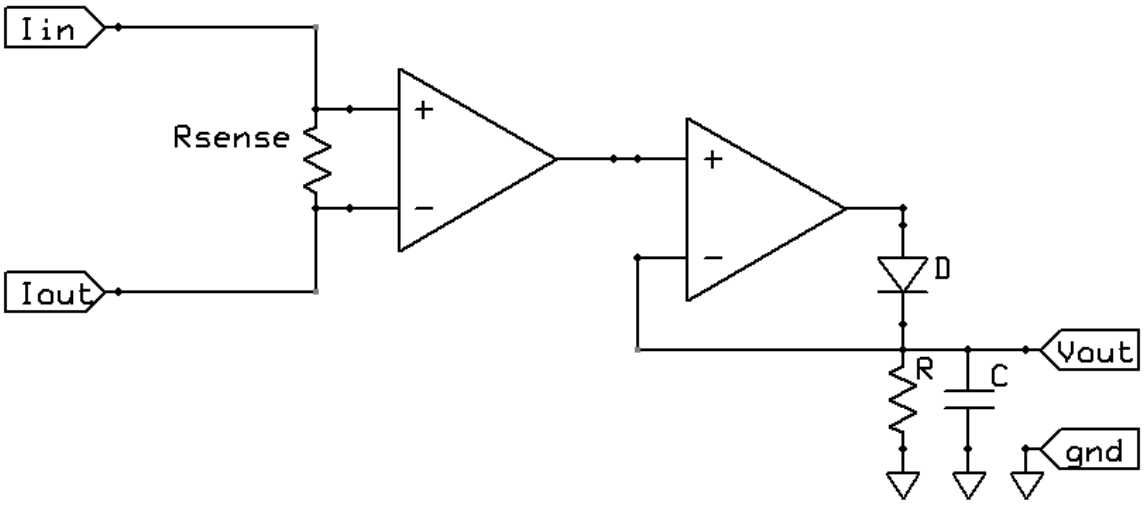


Figure 11: Imag Measurement Circuit

Notice, because current is being measured in this circuit, the input and output ports are labeled Iin and Iout. This circuit will measure positive DC currents or the positive maxima of a sinusoidal input. In implementation, the differential amplifier will require a fairly large gain because the sense resistances must be very small. The sense resistor must be small enough so that the added resistance is negligible in comparison to the load impedance; it is typical that this resistor be on the order of 100 mΩ. When measuring current in this manner, care must be taken to ensure the analog to digital converter (ADC) that is performing measurements at Vout is not being underutilized. The range of currents being measured should produce a range of voltages that cover the entire range of the ADC, otherwise the measurements may be "coarse" if only a small range of the ADC codes are being covered. It is advantageous to adjust the differential amplifier gain so that a typical midscale level measured current produces a voltage that is near the ADC's midscale voltage, which will assure that more of the ADC codes are utilized.

Figure 11 indicates the point in the circuit the current is measured. The current coming out of and going into the source must be equal. If the current is measured coming out of the source, large common mode voltages would not likely be adequately rejected by the differential amplifier. The common voltages coming out of the source are very large compared to the voltage across a small current sensing resistor. If the current

returning to the source is measured, which must be equal to the current leaving the source, the high common mode voltages are avoided. Much more accurate current measurements can be made using this method. Recall that current is measured at this point so a ratio of current and voltage can be used as a control signal.

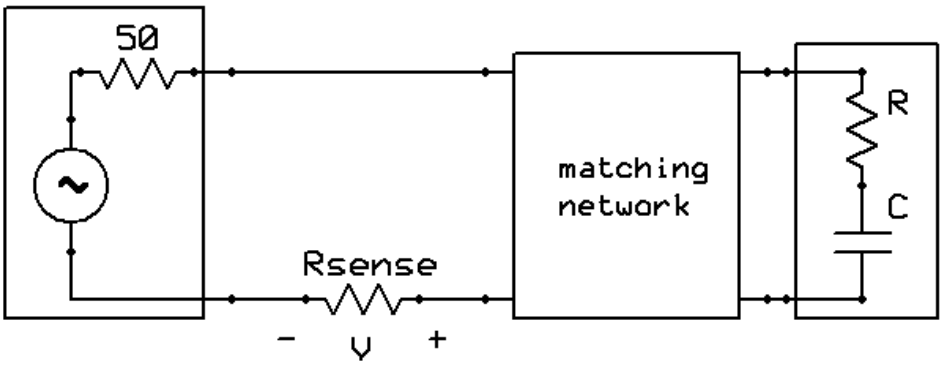


Figure 11: Imag Measurement Point

In this example, I_{mag} will be calculated by converting the voltage measured at Vout in the circuit displayed in Figure . Assume the gain of the differential amplifier A_{diff} is 15 V/V. If the maximum current in a sinusoidal signal is 1 A and is flowing through a sense resistor of 100 mΩ, the maximum voltage across Rsense will be

$$V_{sense} = I_{mag} R_{sense} = (1)(.1) = .1 \text{ V}.$$

This will now be amplified by the gain of the differential amplifier.

$$V_{ampmax} = V_{sense} \times A_{diff} = (.1)(15) = 1.5\ V$$

Now, if some substitutions are made, I_{mag} can be directly calculated based on the V_{ampmax} measurement.

$$V_{ampmax} = \left(I_{mag} R_{sense}\right) \times A_{diff}$$

$$I_{mag} = \frac{V_{ampmax}}{R_{sense} A_{diff}}$$

$$I_{mag} = \frac{1.5}{(.1)(15)} = 1 \text{ A}$$

This calculation can be done by converting the result at Vout with an ADC and performing the numerical calculations with a microprocessor.

2.2.2 Measuring Phase

When a test voltage of $1\angle 0°$ was previously applied to an inductive and resistive load, the resulting current lagged by some angle behind the voltage due to the angle of the impedance. This phase lag can be explained by introducing some differential equations that describe the circuit. The voltage across an inductor is related to the dime derivative of the current multiplied by the inductance.

$$V = L\frac{di}{dt}$$

For this example, a time dependence t is added to the voltage and current.

$$v(t) = L\frac{di(t)}{dt}$$

If a sinusoidal current is applied to a purely inductive load, the voltage will equal

$$v(t) = L\frac{d}{dt}\sin(\omega t) = L[\cos(\omega t)] = L\left[\sin\left(\omega t + \frac{\pi}{2}\right)\right].$$

This means that the voltage will be *leading* the current by $\frac{\pi}{2}$ radians. In a similar fashion the time dependant current can be found.

$$v(t) = L\frac{di(t)}{dt}$$

$$i(t) = \frac{1}{L}\int v(t)dt$$

Supplying a sinusoidal voltage to a purely inductive load will result in a current equal to

$$i(t) = \frac{1}{L}\int \sin(\omega t)\, dt = \frac{1}{L}[-\cos(\omega t)] = \frac{1}{L}\left[\sin\left(\omega t - \frac{\pi}{2}\right)\right].$$

The current is *lagging* the voltage by $\frac{\pi}{2}$ radians, which confirms the result found in the previous voltage calculation. When a resistor is added in series with the inductor, the current can be found using the following ordinary differential equation (ODE).

$$v(t) = Ri(t) + L\frac{di(t)}{dt}$$

Solve for $i(t)$ given $v(t) = \sin(\omega t)$.

$$i(t) = \frac{R\sin(\omega t) - \omega L\cos(\omega t)}{R^2 + \omega^2 L^2}$$

Here, a useful trigonometric property can be applied to understand the relationship the current's phase angle has with respect to R, L and ω.

$$a\sin(x) + b\cos(x) = \sqrt{a^2 + b^2}\sin(x + \varphi),$$

where

$$\varphi = \tan^{-1}\left(\frac{b}{a}\right) + \begin{cases} 0 \text{ if } a \geq 0, \\ \pi \text{ if } a < 0 \end{cases},$$

$$i(t) = \frac{R\sin(\omega t) - \omega L\cos(\omega t)}{R^2 + \omega^2 L^2} = \frac{1}{\sqrt{R^2 + \omega^2 L^2}}\sin\left(\omega t + \tan^{-1}\left(\frac{-\omega L}{R}\right)\right).$$

It is clear from the above expression that the current $i(t)$ will deviate in phase by $\tan^{-1}\left(\frac{-\omega L}{R}\right)$ in an RL network excited by a sinusoidal voltage $\sin(\omega t)$. To verify consistency with previous calculations, the values used in the circuit illustrated in **Error! Reference source not found.** will be applied to this expression. The resulting phase angle is

$$\tan^{-1}\left(\frac{-\omega L}{R}\right) = \tan^{-1}\left(\frac{-(2\pi \times 500 \times 10^3)(30 \times 10^{-6})}{30}\right) = -72.34°.$$

The resulting amplitude is

$$\frac{1}{\sqrt{R^2 + \omega^2 L^2}} = \frac{1}{\sqrt{30^2 + (2\pi \times 500 \times 10^3)^2 (30 \times 10^{-6})^2}} = 10.1105 \times 10^{-3} \text{ A.}$$

Both results are consistent with those found in previous calculations.

It was discussed earlier in the 2.1 Mathematic Background for Impedance Measurement section that if the impedance magnitude Z_{mag} and phase angle θ were measured, the resistance and capacitance or inductance could be determined in a reactive load. To measure phase, a phase detector device can be used. Many types of phase detectors have been designed, each of which has benefits and drawbacks for different specific applications.

Three particular phase detectors will be discussed. All of the detectors are included in the 4046A integrated circuit, which contains many of the essential elements to create a phase-locked loop (PLL).

The first phase detector inside of the 4046A device is an exclusive-or (XOR) gate. This is simply a logic gate that can be used to detect the phase relationship between two digital signals where the phase difference is between 0° and 180°. The XOR gate behaves much like an overdriven multiplier phase detector when the inputs are held at a 50% duty cycle (Wolaver, p. 55). By examining Table 1, it can be seen that the XOR gate at steady state input conditions will produce a pulse train at 50% duty cycle when the inputs differ by 90 degrees. If the pulse train is low-pass filtered to eliminate the frequency components just above DC, the resulting output will be a DC voltage at $\frac{3.3V}{2} = 1.65$ V given that a logic level "1" is represented by 3.3 V. **Error! Reference source not found.** describes the output of the detector for the four possible input combinations.

Table 1: XOR Truth Table

XORin A	XORin B	XORout
0	0	0
0	1	1
1	0	1
1	1	0

Figure 12 illustrates the relationship between the input phase and the DC component of the output voltage.

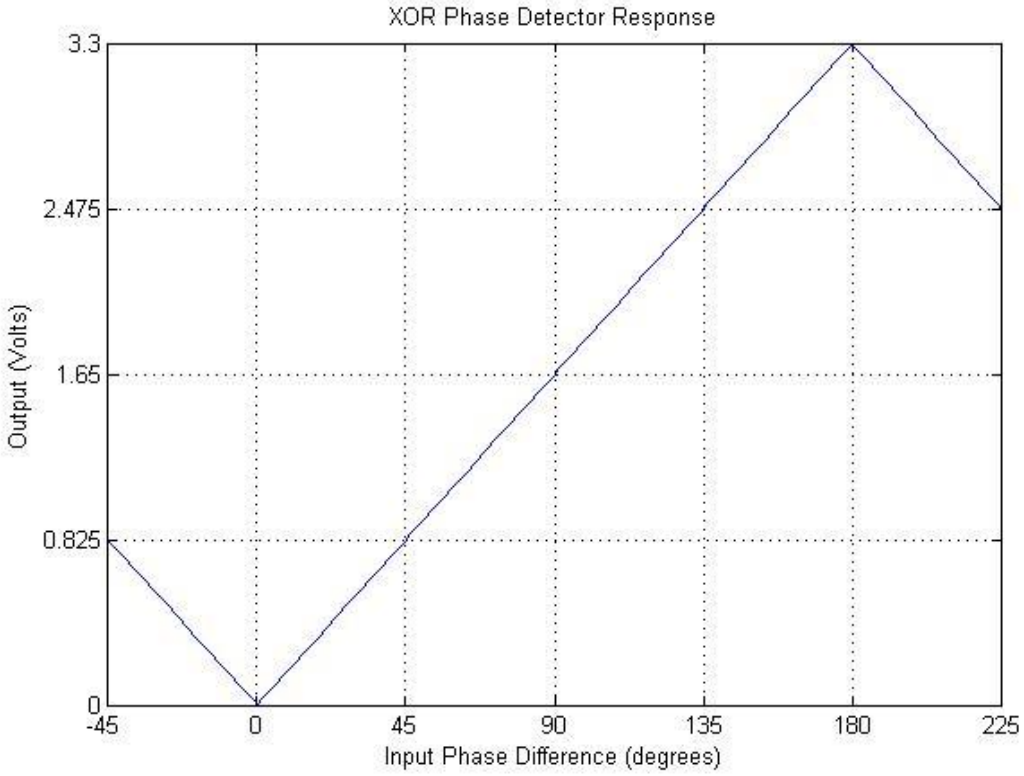


Figure 12: XOR Phase Detector Response

When the inputs deviate from 50% duty cycle, the detectable range of phase becomes limited and a large amount of error is added. This detector has many desirable attributes if the duty cycle of the incoming signals are guaranteed to be a 50%. One way

to achieve this guarantee is to divide the incoming signal's frequency by a factor of two with a divider that is clocked on each rising edge. This process however adds complexity and more devices to the phase detection circuit. The case of added phase error caused by duty-cycle errors is discussed in detail in (Wolaver, p. 58). Other phase detectors are not required to overcome such a constraint when it comes to duty cycle.

Considering Figure 12, the useful range of phases measured by the XOR gate is 0 to 180 degrees. When the input extends beyond this range, the detector's output voltage will "wrap" around to a value equal to a phase being measured in the 0 to 180 degree range. This is not usually desirable in the application of measuring the phase relationship between voltage and current. For instance, if the input phase is -45 degrees, the detector will produce an output identical to if the input phase was +45 degrees. In order to avoid the boundary areas of the detector, the two input signals can intentionally be offset by a certain amount. For the XOR detector, if the input phase relationship was intentionally offset by 90 degrees, the detector will have the 0 degree point moved to half-scale voltage output and the detector could measure between -90 and +90 degrees without wrapping. The ability to measure this range of phases is desirable due to the fact that the phases in an RL or RC network will be within this range. Additionally, if the XOR detector is to be used it must be guaranteed that the input signals are exactly 50% duty cycle to avoid added error and diminished range as well as having the input signals offset by 90 degrees to get the desired boundary avoidance. This requires a considerable amount of extra hardware separate from the XOR gate required to successfully measure phase.

The second phase detector inside of the 4046A device is the RS flip-flop detector. This phase detector is capable of measuring the phase relationship between two digital signals where the difference in phase is between 0° and 360°, double the range of the XOR detector. Another attractive feature of the RS flip-flop detector are its duty cycle restrictions. Because the output is set and reset on the rising edges of the two signals, RS flip-flop detectors are able to detect signals with duty cycles other than 50% with no added error. The state diagram for the RS flip-flop detector is displayed in Figure 13.

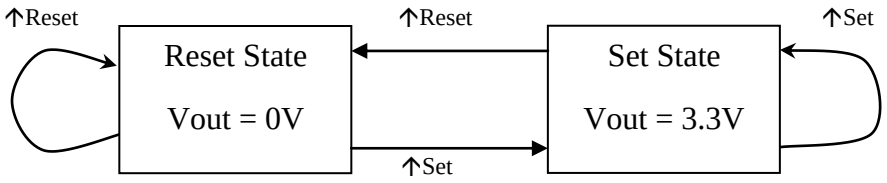


Figure 13: RS Flip Flop State Diagram

From this diagram, it is apparent that the state is changed by a rising edge on the set or reset inputs. If the DC component is considered, as with the XOR gate, an input of two exactly in-phase signals results in a race condition between "set" and "reset" and the output signal will be indeterminate. In this race condition, the output is either pulsed high for an infinitesimally short amount of time, or the output is set high for the duration of the cycle of the input signal. As seen in Figure 14, if the phase is exactly 0 degrees, the output lies on a discontinuity and the output is unknown. If the inputs are 180 degrees out of phase, the detector is in the "set" and "reset" states equal amounts of time, resulting in an output of 1.65 V, or 50% of 3.3 V. The full output response is indicated in Figure 14.

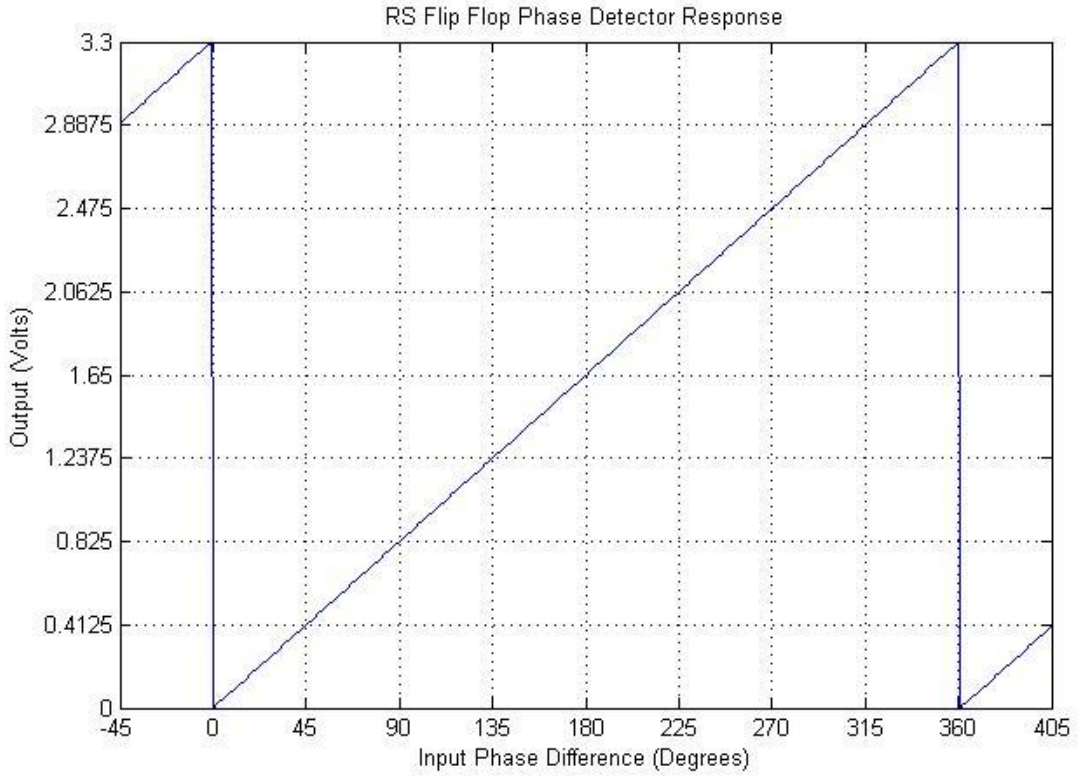


Figure 14: RS Flip Flop Phase Detector Response

In Figure 14 it is clear that the RS flip flop has a boundary problem similar to the XOR phase detector. When the input phase is less than 0 degrees, the output will wrap and produce a false or misleading result. For example, if the input phase was -45 degrees, the output appears as if the input was 315 degrees. This phase relationship may be true depending on which input is the reference input, but is false if the same input is used as a reference for both positive and negative phases. The same phenomenon occurs when the phase is greater than 360 degrees. To avoid these boundaries, the input phase can be intentionally offset, like with the XOR gate, but by 180 degrees. This will shift a 0 degree input phase output to midscale (1.65 V). A 180 degree phase shift is achieved if one of the signal inputs is simply inverted. Because the RS flip-flop detector has a wide phase measurement range, a large portion of the useable range will not be utilized (50%) in this application due to the fact that RC and RL circuits have current and voltage phase relationships that range between -90 and +90 degrees. One method that can be used to

solve this problem is to set the ADC's -Vref and +Vref input to the desired boundaries of the detector.

Finally, the third phase detector in the 4046A PLL device is a dual D flip-flop detector with a tri-state output stage, sometimes called a "Z-state" phase detector. This detector is different than the previously discussed designs simply because the output stage has three states (high, low and tri-state). The D flip-flops activate current sources in the tri-state output stage that either source, sink, or produce a zero current state. The main advantages of this detector are brought forth when the detector is used in a PLL circuit because it provides the ability to create a near-zero static phase error PLL using a passive loop filter. These benefits are not directly needed in the application of simply measuring the phase between two signals. A loop filter is not used and no VCO is controlled, so the advantages are left unutilized. Thus, only the XOR gate and the RS flip flop detectors are considered.

The RS flip flop detector was chosen due to its simplicity in implementation relative to the XOR detector despite the problem with the unused measurement range. Compared to the XOR gate, the amount of additional hardware required to condition the incoming signal for the RS flip-flop is much less, making the detector very attractive when considering hardware implementation.

In order to measure the phase relationship between the voltage and current, the signals must be conditioned so that the RS flip-flop phase detector can be used. The phase detector, being a logic device, is triggered on the rising edge of signals, and therefore the incoming signal must contain these edges. The voltage and current signals to be measured must be square in nature and must possess sharp edges to change the state of the phase detector. If the signal is made up of a single frequency with little to no DC offset, a comparator will be able to convert the signal into a 50% duty-cycle square-wave. In this application, the comparator's output is simply 0 V when the signal voltage is below 0 V, and 3.3 V when the signal is greater than 0 V, effectively measuring the sign of the Voltage. This can be accomplished by setting the comparator's compare voltage to

0 V, or ground potential. To measure the sign of a current, a small sense resistor can be added in series with the load and a voltage measurement across the resistor indicates the current. A comparator can be placed with its two inputs on either side of this resistor to measure the sign of the current in the same manner the sign of the voltage is measured. If the current is flowing through the sense resistor in a certain direction, the voltage on one side of the resistor will be greater than the other and the comparator will "compare" the two voltages, switching its output high or low depending on the orientation of the inputs. This creates a comparator circuit that transitions its output when the current changes from one direction to the other.

Earlier, it was suggested that the input to the RS flip-flop phase detector can be intentionally offset by 180 degrees. This is done very simply by changing the orientation of the comparator inputs so that if a positive current is flowing through the sensing resistor, the comparator produces a low output and vice versa. This accomplishes the 180 degree phase shift without adding any hardware. Below is a simplified circuit indicating the configuration of the mentioned phase measurement circuit including the orientation of the comparators. Notice that Rsense is placed in series with the load on the low side. This is crucial in prevention of large common modes on the two inputs of the current measuring comparator. If the sense resistor was placed before the load, the common mode will not be adequately rejected and the resulting waveform will be invalid.

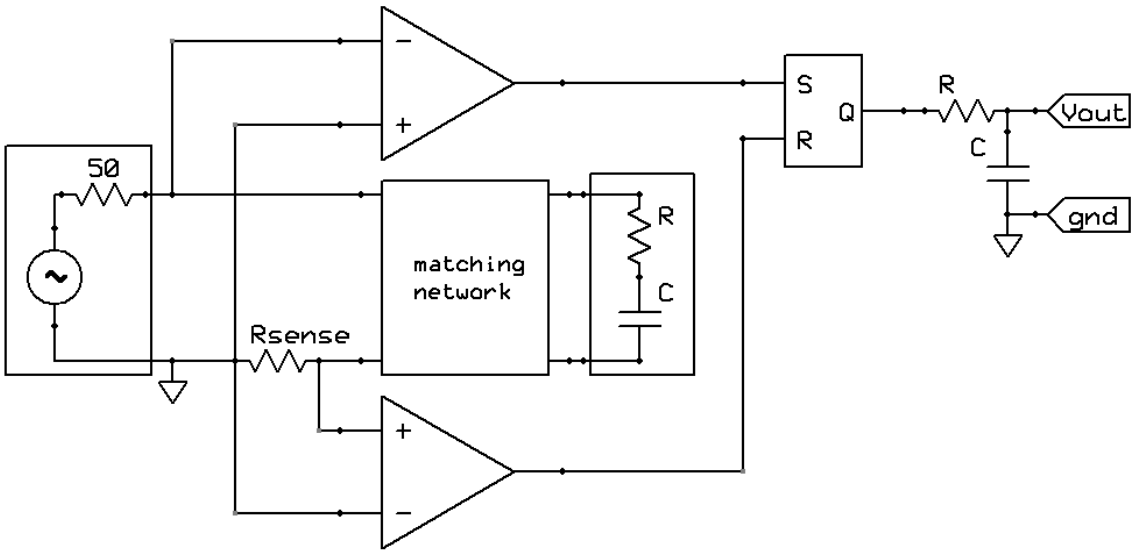


Figure 15: Phase Measurement Circuit

The phase detector device that is receiving the two comparator outputs is the RS flip flop phase detector. The phase detector will produce a digital signal which is then filtered by the resistor and capacitor that is connected to its output. The RC filter should be designed in such a manner that the high frequency components contained in the digital signals are reduced so that only the DC component remains. However, the filter must also allow the signal to change at a fast enough rate so that the phase can be tracked at a useful rate of change, which is determined by the measurement application.

2.2.3 Measuring Frequency

After an impedance is measured, finding the value of the reactive element requires knowledge of the frequency at which the measurement was made. Recall the formula for the impedance of an inductor and capacitor.

$$jX_L = j\omega L$$

$$-jX_C = \frac{1}{j\omega C}$$

The above measurements of Z_{mag} and the phase angle θ result in the ability to calculate jX. If jX is negative, the formula for calculating capacitance is used. Conversely, if jX is

positive, the formula for calculating inductance is used. To find the reactive element's value, simply solve for L and C in the above equations.

$$L = \frac{X_L}{\omega}$$

$$C = \frac{1}{\omega X_C}$$

Obviously, if the values for L and C are to be found, the value for ω must be known. In this application, the chemistry researchers could enter the value for the input signal frequency, but this would involve unnecessary human interaction. One design goal that has been determined is to reduce human interaction as much as possible to create an autonomous system. Furthermore, if the frequency was entered incorrectly or changed without update, any subsequent calculations involving frequency will be incorrect. Thankfully, measuring frequency with this device to a high degree of accuracy is a simple task.

One method of measuring frequency is to use a frequency counter. This is a digital device that counts clocks or edges within a specific time period. The number of clocks counted within the time period directly indicates frequency. The reference time period is easily generated by a highly accurate crystal oscillator. Low-cost crystal oscillators can have errors in the range of $\pm$ 20 ppm. The oscillator used to provide the clock to the microprocessor in the device at 16 MHz has a $\pm$20 ppm accuracy. The microprocessor will count pulses from the circuit that converts the sinusoidal signal voltages into a square pulse train located in the phase detection circuit. These square pulses will be read by an external clock input on the microprocessor's timer module and will increment a counter on each pulse. Meanwhile another counter will be incrementing at each pulse of the 16 MHz oscillator clock that has been divided by 16 to create a 1 MHz clock. When the 1 MHz clock has counted to 1 million, taking one second to do so, the number of clocks counted from the external clock input is stored to memory. The number of clocks counted during the one second time period directly indicates the

frequency. If there are 1 million reference clocks in one second, and the external pulse count result is 800,000, the resulting frequency is 800,000 Hz. The reference time period limits the range of frequencies that can be measured and the resolution of frequencies that can be obtained. The frequency of the signal used to measure impedance should be periodically checked so that any performed calculations will be accurate.

Chapter 3

Maximum Power Transfer

This chapter will introduce the methods required to calculate and deliver maximum power into a reactive load.

3.1 Impedance Matching

When the load impedance is known, several simple steps can be taken to achieve maximum power delivery. First, the maximum power transfer theorem will be introduced. The average power into a load can be found using the equation below.

$$P_{avg} = I_{rms}^2 R_L = \frac{1}{2} I_{mag}^2 R_L$$

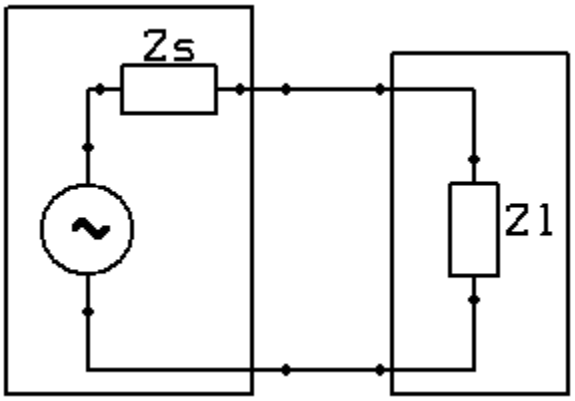


Figure 16: Reactive Source and Load Impedance

The current I_{mag} can be expressed as

$$I_{mag} = \left(\frac{V_{mag}}{Z_s + Z_L}\right).$$

substituting,

$$P_{avg} = \frac{1}{2} I_{mag}^2 R_L = \frac{1}{2}\left(\frac{V_{mag}}{Z_s + Z_L}\right)^2 R_L.$$

Impedances are made up of a complex and a real part $R \pm jX$. The complex form of impedance is substituted for Z.

$$P_{avg} = \frac{1}{2}\frac{V_{mag}^2 R_L}{(R_s + R_L)^2 + (X_s + X_L)^2}$$

By inspection, P_{avg} will be maximized when the denominator of this equation is minimized. One way to minimize the denominator is to have $X_s = -X_L$ to cancel out the reactive term entirely, leaving just the resistive terms.

$$P_{avg} = \frac{1}{2}\frac{V_{mag}^2 R_L}{(R_s + R_L)^2}$$

Now, if this equation is inspected, the relative maxima can be found by taking the partial derivative with respect to R_s, setting the equation to zero and solving for R_L. This will reveal the value of R_L that maximizes P_{avg}.

$$\frac{dP_{avg}}{dR_L} = \frac{d}{dR_L}\left(\frac{1}{2}\frac{V_{mag}^2 R_L}{(R_s + R_L)^2}\right) = \frac{1}{2}\left(\frac{V_{mag}^2}{(R_s + R_L)^2}\right) - \left(\frac{V_{mag}^2 R_L}{(R_s + R_L)^3}\right) = 0$$

This equation is satisfied when $R_L = R_s$. This means that maximum power will be delivered to the load when the source and load reactance cancel and the real resistances are equal. When this condition is met, the source and the load are complex conjugates of each other. It is also interesting to note that an ideal voltage source with a series resistance will at most deliver only half of its total power into the load resistance! In other words, the best situation possible is to dissipate half of the system's power in the source resistance and only half of the available power into the load because of the $\frac{1}{2}$ term in the P_{avg} equation.

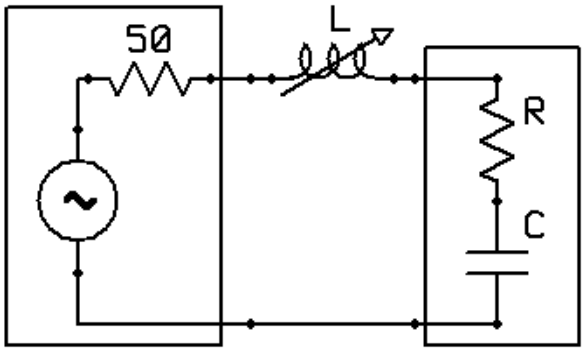


Figure 17: Variable Inductor in Series with an RC load

The above analysis reveals several ways to increase power delivered to a reactive load. If the load impedance consists of a resistance and a capacitance, an inductor of equal reactance to the capacitor can increase the power delivered to the load regardless of the real part of the load's impedance. If a variable inductor is placed in series with the load, as the inductance changes, the current through the entire circuit will be shifted by a varying degree. The capacitor causes current to lead the voltage in phase and the inductor causes current to lag the voltage. When the inductor shifts the current to the negative angle by the same amount that the capacitor shifts the current to the positive angle, the current is now in phase with the voltage. When this condition occurs, the two reactive elements are cancelled and the load appears as a "real" resistance to the source. This will increase P_{avg} because the $(X_s + X_L)^2$ term is now equal to zero, which causes the denominator in the P_{avg} equation to decrease. If the relationship between phase and the series inductance is analyzed, a useful control technique is revealed.

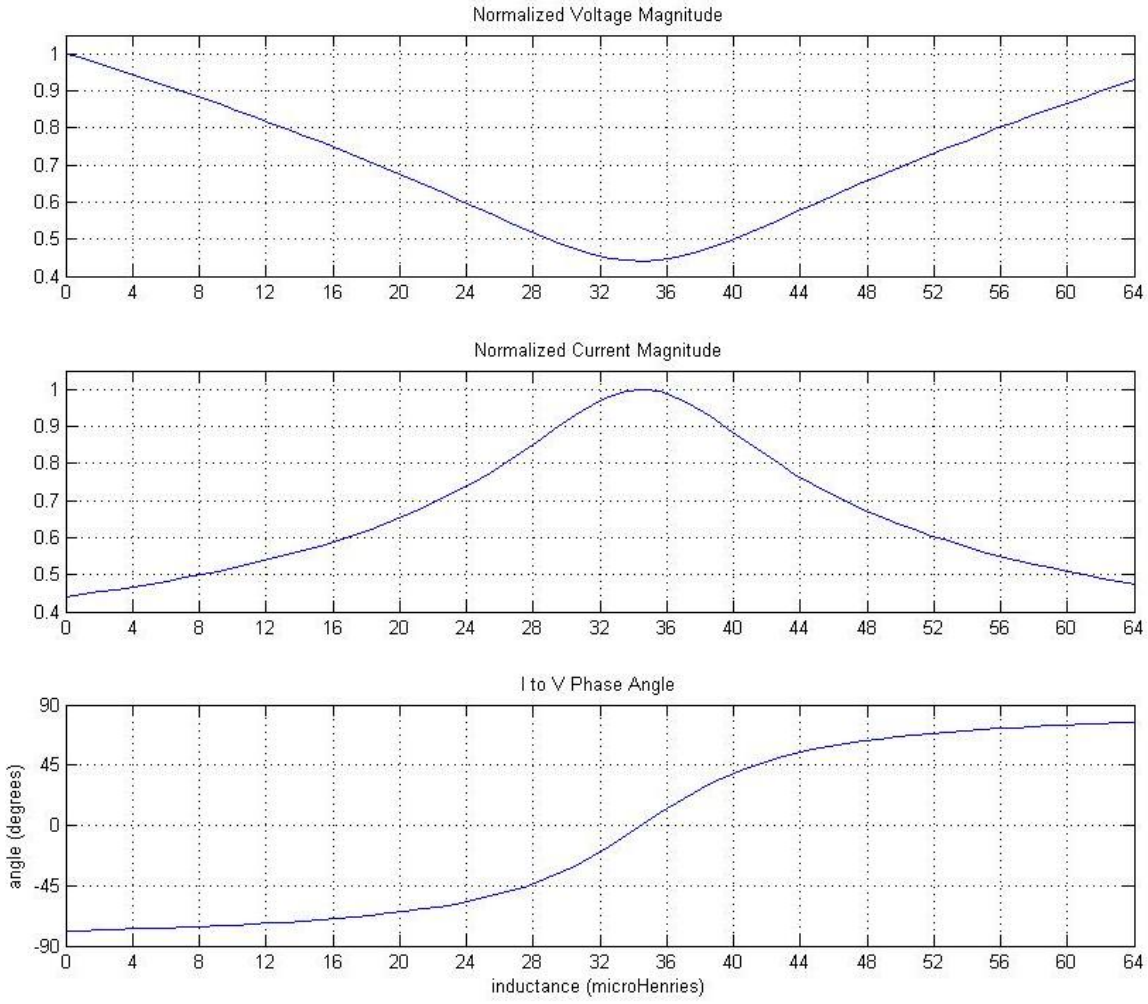


Figure 18: Voltage, Current and Phase vs. Inductance

Figure 18 shows a scenario where the load capacitance has been set to 1.5 nF, resistance to 30 Ω, the frequency to 700 kHz, and the series inductance swept from 0 to 64 μH. The voltage is measured across the node between the variable inductor and the 50 Ω resistor, and the current is constant through the entire circuit because there are no branch currents. Note that both the current and the voltage change more than 50% from their initial value. In the area where the voltage is minimized and current is maximized, the phase transitions from a negative to a positive value. As the phase passes through zero degrees, the voltage and current ratio change as if there was only a 30 Ω resistor present in the load. At this point, the two reactive elements are cancelled. Power has been

increased, but power transfer is not yet completely maximized until the load resistance is equal to the source resistance. In this example, the load resistance is $30\ \Omega$ and the source resistance is $50\ \Omega$. The power below efficiency maximum is calculated as

$$P_{ratio} = \frac{power\ with\ load\ R_{Lx}}{power\ with\ 50\ \Omega\ \text{load}\ R_L} = \frac{R_{Lx}(R_s + R_L)^2}{R_L(R_s + R_{Lx})^2}$$

$$P_{ratio} = \frac{30(50+50)^2}{50(50+30)^2} = \frac{15}{16} = 93.75\%.$$

If the load resistance matched the $50\ \Omega$ source resistance, 6.25% more power can be delivered to the load. Several methods can be used to actually "transform" the load resistance into the desired $50\ \Omega$, which will be discussed in more detail later.

Note the value of the phase as the inductance is swept in Figure 18. It must be reiterated that at the point where the phase is at or near $0°$, the power is maximized and therefore the inductance value at this point is of interest. This inductance value can be calculated as follows.

$$X_{series} = -X_L$$

$$j\omega L = -\frac{1}{j\omega C}$$

$$L = \frac{1}{\omega^2 C}$$

In this particular situation, the required inductance value to cancel the capacitor is

$$L = \frac{1}{(2\pi \times 700 \times 10^3)^2 (1.5 \times 10^{-9})} = 34.45\ \mu\text{H},$$

which is consistent with the plot. The phase angle passes through $0°$ just before 35 µH.

If a device was created that could provide a continuously variable inductance, the phase angle could be used as a control signal to adjust the inductance value in a closed-loop feedback control system. To cancel out the series capacitance, if the phase is less

than zero, more inductance is required. If the phase is greater than zero, less inductance is required. The phase angle magnitude can be used as an error signal of varying amplitude. If the phase is only slightly negative, a slight increase of the inductance is required, and so on. After the phase converges to a value near zero, the reactance has nearly canceled, and the inductance should maintain a value that can track variations that may occur in the load impedance.

The design of such a system includes an electronically controllable variable inductor and a device that calculates the required inductance based on the phase measurements. Assume that a continuously variable inductor exists and can provide infinite inductance values within a set range. If the phase is known and used as a control signal, no other measurements are required to cancel the load reactance. The only calculations that must be made are related to the direction that the inductance should be changed and by what amount. In the application of ultrasound transducers and chemistry research, the impedance of the load will not change rapidly, and the nature of the research requires a circuit that will be very stable and react very slowly to changes over time. In such a case, after a suitable inductance has been found, the update rate can be slow, possibly on the order of a half second to seconds, so that no large or sudden changes are made to the power delivery during tests, data collection or use in the field. With this information, a feedback control topology can be analyzed.

A simple and common feedback control topology is the proportional integral derivative controller, or PID controller. This is a closed-loop feedback system that will, under stable conditions, servo or converge the feedback variable to equal a "set-point" that is defined by the user. Such a system is very easy to implement. For a full PID device, several multipliers, an integrator, a differentiator and two summing blocks are required as indicated in the image below.

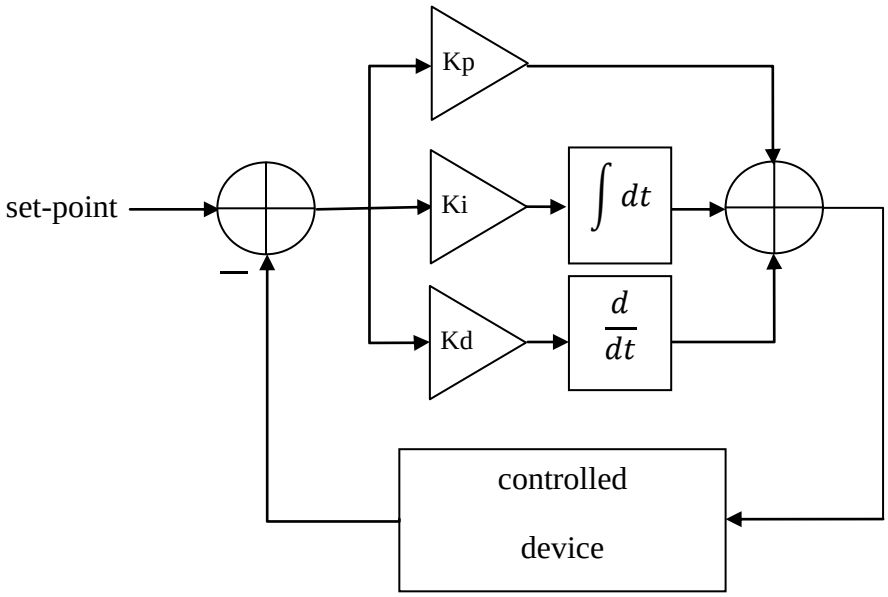


Figure 19: PID Controller Block Diagram

The "controlled device" block represents the variable inductor, which is being controlled by the input signal. The output of the controlled device is the phase measurement, which is fed into the subtracting block. The amplifiers or multipliers each multiply the result of the subtraction block by predefined "coefficients", Kp, Ki and Kd, each weighting the signal accordingly before it passes into the proportional, integrator and differentiator stages. Notice the leg containing Kp lacks the second element that the integrator and differentiator legs posses. The proportional leg simply amplifies the feedback subtracted from the set-point and sends the result to the summing block. The integrator when implemented digitally is simply an accumulator. Each time step the integrator adds the current value present at the input to the sum of all of the previous values encountered. In most cases the sum is never cleared and error accumulates forever. If the accumulated error is a positive value and negative errors start to present themselves at the input to the integrator, the error sum will become less positive and eventually become negative.

The integrator section when used in this configuration is useful in "slowing down" the response of the system to errors due to the pole it adds to the transfer function of the system. By slowing down the response, more stability can be achieved at the expense of initial acquisition time. To achieve this effect, the coefficient associated with the integrator leg, Ki is made very small so that small amounts of error are accumulated in each time step. Upon power-up of the device, error can be quite large. If the system is slow responding, it will take some time to accumulate enough error to make the necessary corrections to servo or correct the system to the set-point.

The differentiator is also simple to implement digitally. A differentiator by nature calculates the slope of the input. To do this the differentiator needs to "remember" the previous element and take the difference between the current and previous element.

The PID controller can operate with any combination of these elements, with each one providing some characteristic to the control loop. For example, if just the "I" portion is implemented, or Kp and Kd are set to zero, the only nonzero result remaining at the summing block will be the result of the integrator leg. The integrator can be set to accumulate error very slowly by setting Ki to a small number. If the input phase is negative, a very small negative Ki coefficient will slowly accumulate positive error that will be presented directly to the variable inductor. The slowly increasing positive error will tell the variable inductor to slowly increase in inductance value, much like the situation shown in Figure 18, when the phase angle is less than zero. After some time, the phase angle will become smaller due to the inductance gradually cancelling out the series capacitance. The accumulated error will become less and less, and the inductance will slowly approach the value that cancels out the capacitor. At the point that the correct inductance is found, the accumulated error from previous inductance values will still be present, and the control system will "overshoot" the correct value and start introducing positive phase angles, which will be accumulated as negative error. The negative error will be added to the accumulated error and gradually decrease its value until it becomes negative, causing the inductance to decrease again until it undershoots the correct inductance value as it passes from negative error values to positive ones. This will

continue to occur as the correct inductance is converged upon. This process of undershooting and overshooting again and again is not exactly desirable. A simple method to correct a convergence problem in an integrating control loop is to create a "window" of error values that set Ki to zero and clear the error accumulator. When the control loop finds an inductance value that causes the error to be within a 2 degree tolerance, an acceptable inductance has been found and the system should stop adjustment. When the Ki coefficient is set to zero and the error accumulator is cleared when the error is in this tolerance window, the inductance control signal will not be changed until the error exceeds the 5 degree boundary of acceptability, the load impedance and the variable inductance is allowed to change slightly without correction. After the phase angle changes enough to cause the phase to exit the 5 degree boundary, the Ki coefficient is reset to its original value, and error will again start to accumulate in the integrator. Possible reasons for phase angle variations are changes in the load impedance and changes in the actual inductor value.

The methods to maximize power transfer have involved cancelling the load's reactance using a variable inductor. Cancellation of the load's reactance will dramatically increase the power delivered to the load. It has also been shown that if the real part or resistance of the source and load are equal, the power will be further increased. It was shown in the example associated with the circuit illustrated in Figure 17 that the power in this circuit can be increased another 6.25% if the resistances are equal as well as the reactive elements cancelled. To do this, the impedance can be "transformed" by a reactive network. An adjustable reactive network can be used to both eliminate the load's reactance and transform the resistance to the required 50 Ω. First, some mathematic background must be presented. The following example closely follows Jack Smith's example in "Modern Communication Circuits" (Smith, 1997).

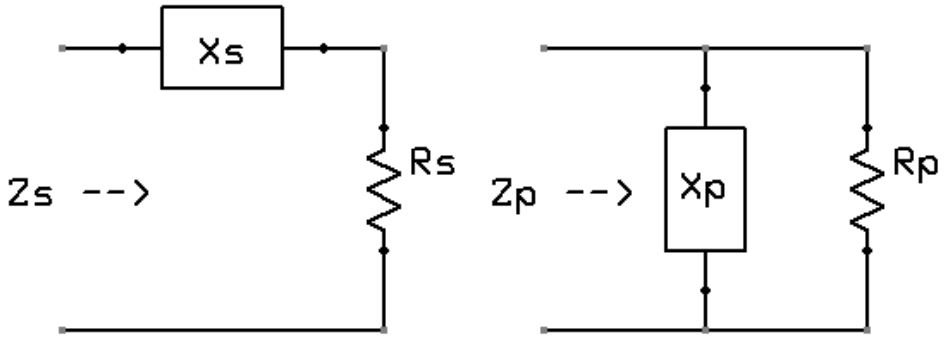


Figure 20: Parallel and Series Reactive Networks

In Figure 20, Zs and Zp are defined as

$$Z_s = R_s \pm X_s$$

$$Z_p = \frac{\pm R_p j X_p}{R_p \pm j X_p} = \frac{R_p X_p^2}{R_p^2 \pm X_p^2} \pm j \frac{X_p R_p^2}{R_p^2 + X_p^2}$$

The real and imaginary parts must equal, R_s and X_s can be defined as

$$R_s = \frac{R_p X_p^2}{R_p^2 \pm X_p^2}$$

$$X_s = \frac{X_p R_p^2}{R_p^2 + X_p^2}$$

Similarly R_p and X_p can be defined as

$$R_p = \frac{R_s^2 + X_s^2}{R_s}$$

$$X_p = \frac{R_s^2 + X_s^2}{X_s}$$

To illustrate the usefulness of these equations, an example will be demonstrated. A circuit diagrams are illustrated in Figure 22 and Figure 23 that correspond with the example. The frequency of operation is set to 800 kHz. First, the parallel resistance is found.

$$R_p = \frac{R_s^2 + X_s^2}{R_s} = \frac{30^2 + (-132.6)^2}{30} = 616\ \Omega$$

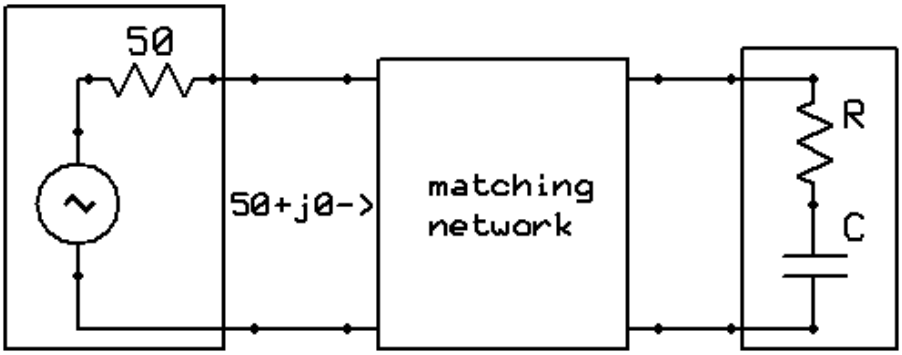


Figure 21: Impedance Transformation with Reactive Matching Network

Because the parallel resistance is found to be much higher than $50\ \Omega$, the matching network must reduce this value to $50\ \Omega$. The objective of the matching network is to deliver maximum power to the load elements, so adding a parallel resistor would not be appropriate because the resistor will dissipate power. However, if R_p can be forced to $50\ \Omega$ by X_s^2 in the R_p equation, the correct impedance level can be achieved.

$$R_p = \frac{R_s^2 + X_s^2}{R_s} = 50 = \frac{30^2 + X_s^2}{30}$$

$$X_s = \pm\sqrt{R_s(R_p - R_s)} = \pm\sqrt{30(50 - 30)} = \pm 24.49$$

An element must be added so that the series reactance of the circuit is equal to ± 24.49. The process to find this element is shown below.

$$\frac{1}{j\omega C} + jX = jX_s$$

$$-132.6 + X = \pm 24.49$$

$$X = 132.6 - 24.49 = 108.11, \text{ or}$$

$$X = 132.6 + 24.49 = 157.1.$$

Because the reactance X found is positive, an inductor with a reactance of either $108.1\ \Omega$ or $157.1\ \Omega$ should be added in series with the load. The inductance value is calculated below.

$$L_s = \frac{X}{\omega} = \frac{108.11}{2 \times \pi \times 800 \times 10^3} = 21.5 \times 10^{-6} = 21.5\ \mu\text{H}$$

$$L_s = \frac{X}{\omega} = \frac{157.1}{2 \times \pi \times 800 \times 10^3} = 31.25 \times 10^{-6} = 31.25\ \mu\text{H}$$

If a $21.5\ \mu\text{H}$ or a $31.25\ \mu\text{H}$ inductor is added in series, the parallel resistance will become $50\ \Omega$, and the parallel reactance can be found using the equation for X_p. Recall that X_s has been found to be ± 24.49.

$$X_p = \frac{R_s^2 + X_s^2}{X_s} = \frac{30^2 + (\pm 24.49)^2}{\pm 24.49} = \pm 61.24$$

Here a choice must be made because two valid answers exist for the element to be placed in parallel with the load. If the parallel reactance is chosen to be $j61.24\ \Omega$, a $-j61.24\ \Omega$ element, or capacitor must be used to cancel out the reactive term leaving just a real $50\ \Omega$ remaining. Conversely, if X_p is chosen to be $-j61.24\ \Omega$, a $j61.24\ \Omega$ element, or inductor must be used to cancel the reactive term. Depending on which element is chosen, the corresponding L_s that used the positive or negative X_s value must be used. The two possible parallel elements are shown below.

$$L_P = \frac{X_P}{\omega} = \frac{61.24}{2 \times \pi \times 800 \times 10^3} = 12.2 \times 10^{-6} = 12.2\ \mu\text{H}$$

$$C_P = \frac{1}{\omega(X_p)} = \frac{1}{2 \times \pi \times 800 \times 10^3 \times 61.24} = 3.24 \times 10^{-9} = 3.24\ \text{nF}$$

Below is an illustration of the two possible networks that create the required impedance transformation. Both networks transform the load into the desired $50 + j0\ \Omega$ required for maximum power transfer.

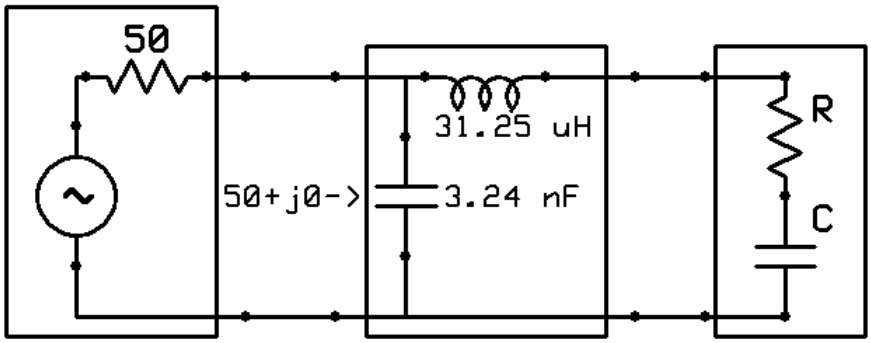


Figure 22: Impedance Matching Solution 1

Here, $R = 30\ \Omega$ and $\mathrm{C} = 1.5$ nF $(-\mathrm{j}132.6\ \Omega)$. The series inductance and capacitance have been calculated to be 31.25 µH $(+\mathrm{j}157.1\ \Omega)$ and 3.24 nF $(-\mathrm{j}61.24\ \Omega)$. Recall, the frequency used in this example is 800 kHz.

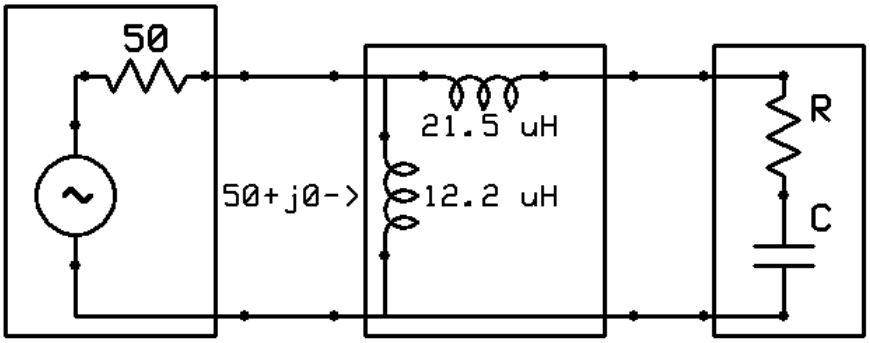


Figure 23: Impedance Matching Solution 2

Figure 23 has the same load as in Figure 22. Here, the matching network consists of two inductors. A series inductance and parallel inductance have been calculated to be 21.5 µH $(+\mathrm{j}105.11\ \Omega)$ and 12.2 µH $(+\mathrm{j}61.24\ \Omega)$.

It is up to the designer to determine which network is the more appropriate for the application. The matching circuit used in Figure 22 contains a capacitor and an inductor

to create the appropriate impedance transformation. In the application involving a variable load impedance, variable impedance matching elements are required to provide matching conditions to a range of load conditions. One disadvantage of the circuit in Figure 22 is the lack of DC path to ground from the source. If the source is AC coupled, which is a distinct possibility, there will be no DC path to ground because each DC current path is blocked by a capacitor. If there is any DC component in the signal source, this DC component will translate directly to measurement errors resulting from DC offset. The circuit illustrated in Figure 23 is more attractive. An inductor will short any DC component to ground, which will make the system insensitive to whether the source is AC or DC coupled. Another benefit to this circuit is that because the circuit must be variable, two identical variable inductors can be used.

The design must be created in hardware, so a variable inductor can be developed for the series element and duplicated for the parallel element. The circuit that contains the capacitor in the matching network must have two different types of variable elements, potentially making design and debugging more costly. If two variable inductors are used, the inductors used in the design can likely be purchased with a quantity discount, reducing the cost of the system.

Because the matching network must accommodate varying load impedances with a finite range of inductor values, only a given range of impedances can be matched with a given set of inductors. The upper bound of the range is set by the maximum capacitive reactance seen in the load. If the reactance is a large negative value (small capacitance, low frequency or both) then the required inductance to cancel the reactance will be very large, possibly so large that the variable inductor cannot produce enough inductance to satisfy the condition. Also, if the calculated variable X_s is *greater* than the reactance in the load, a negative reactance must be added (capacitor). The lower bound will be determined by a non-capacitive or inductive load reactance. The series variable inductor adds positive reactance so it will be likely if the load is inductive, the matching condition will require a capacitance to cancel the positive reactance present in the load.

When measuring phase, now that the matching network is included in the design, the phase relationship between the voltage measured *before* the matching network and the current *returning to the source* will yield the desired control signal, which can be driven to a set-point of zero degrees. The voltage and current magnitude should also be measured at these points. The current *returning to the source* through the ground node and the voltage across the *matching network and load* will be the quantities used in the required calculations. The combination of the matching network and load must appear to be $50\ \Omega$ when viewed from the source as discussed above. The reason the current returning to the load is measured has to do with common mode voltages. Since the current leaving the source and returning to the source must be identical, the current returning to the source is better to measure. The common mode voltages presented to the differential amplifier discussed earlier will much smaller, allowing the amplifier to measure currents with less error.

Because two variable inductors are to be used in the matching network, the feedback control system must take into consideration the impedance magnitude in addition to phase. When the phase is cancelled by the series inductor, a smaller parallel inductance will cause the load to increase in apparent real resistance and vice versa. If the series inductor is always tuning out the load's reactance using the mentioned "I" controller, then slowly changing the parallel inductor will allow the load's apparent real resistance to be varied. The key is having the series reactance tuned out quickly enough or the parallel inductance to be varied slowly enough so that the series inductance control system converges before the parallel inductance control system makes a decision about which way to change the inductance value.

To make this happen, the parallel inductor control system increments a variable or tallies the number of measurements taken that the impedance magnitude is above or below a window of acceptable values. For example, if the impedance magnitude is below $45\ \Omega$ the tally is decremented by one and if the magnitude is above $55\ \Omega$ the tally is incremented by one. When the tally reaches a threshold of, for instance 5, so that the impedance magnitude is known to be below the range of acceptable values, the

inductance value is decreased by a certain amount, and it is increased if the tally reaches -5. After the tally of ± 5 is reached, the parallel inductance is updated accordingly, and the tally is reset to zero, so that the series inductance has time to servo the phase to zero. If the Impedance magnitude lies within the window of acceptability, the tally remains constant but is not cleared. The tally threshold and the acceptable impedance magnitude window can be changed to make the system more or less sensitive to changes in impedance magnitude. The control system responsible for varying the parallel inductance is similar to the series inductance control system in that the error is "accumulated" or "integrated" over time.

3.2 Variable Inductor Design

A matching network comprised of two variable inductors has been determined to be the most suitable solution. A variable inductor must be designed that will be able to provide the required inductance values to match a wide range of loads. Ideally, the inductor should be digitally controllable so that a low cost microprocessor can take measurements required to match and can adjust the inductance directly. One possibility is to have a bank of inductors that can be added together with switches or relays. The inductance values could all be equal or have some range of values depending on the design. Figure 24 illustrates this concept.

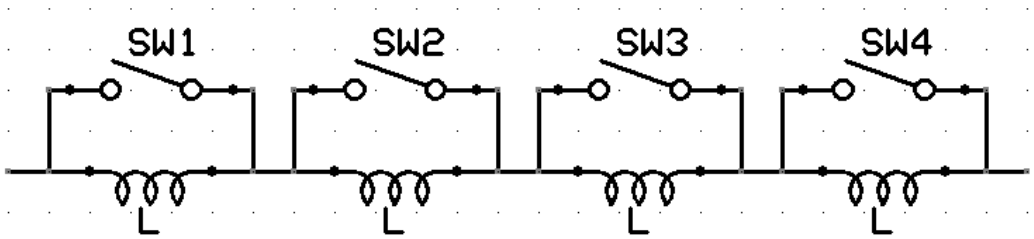


Figure 24: Variable Inductor Using Equal Value Inductors

When a switch is opened, the current is forced to flow through the inductor, effectively adding it in series to the rest of the circuit. When a switch is closed, the current will follow the path of least resistance and flow through the switch, the switch is a short circuit. This effectively removes the inductor from the series circuit. Depending on the switch position, the inductance in the above depiction is able to range from 0 to 4

times the value of L. One drawback to this design is that fifteen inductors and switches would have to be used to achieve an inductance range of, for example, 0 to 15 times the value of L. If the inductors had different values, the range of inductances could be increased with the same number of switches and inductors as the design previously mentioned. This concept is illustrated in Figure 25.

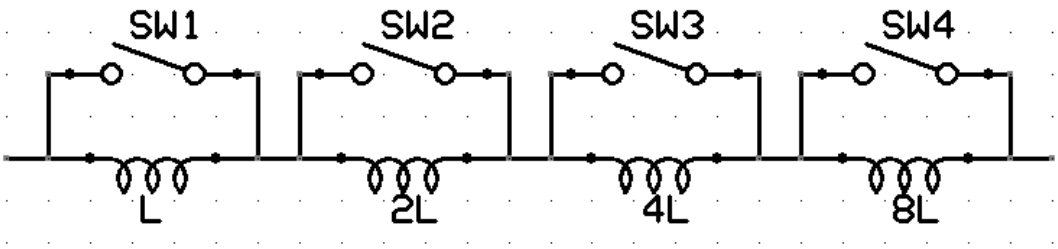


Figure 25: Variable Inductor Using Binary Progression of Inductances

When the inductors are spaced using a "binary progression", each inductor value is twice that of the next smallest value. This allows the inductance range to be from 0 to $2^N - 1$, where N is the number of inductors used in the design. In the above example, the inductance would be variable between 0 and 15 times the value of L. If the required inductance value was calculated inside a microprocessor to be 10L, the binary pattern that represents the number 10 will switch the correct switches that make the 10L inductance value. In the previous example, where the inductance values were all equal, it takes 10 inductors to make the value 10L.

With the binary progression of inductance values, the number of physical inductors needed to create 15L is dramatically reduced to 4. With only 4 inductors, any value between 0 and 15L can be created with steps of 1L. As intriguing as it sounds, a downfall to this arrangement exists if *accurate and precise* inductance values are needed. Inductors by nature are not precision devices. An inductor is simply a coil of wire, usually wrapped around a ferrite core. The mechanical variations in the manufacturing process frequently yield a 10-30% tolerance in the inductance value. Another contributor to inductance variation is the thermal heating of the ferrite core and the windings.

Inductors are specified a tolerance value given a specific temperature range and are allowed to vary within the tolerance as long as the temperature stays in the specified range. The ferrite core and windings can grow hotter with the amount of current flowing through the inductor. A large alternating current will induce large magnetic fields in the inductor's ferrite core, which will cause warming when current levels grow very high. High currents flowing through a wire, which has a very small but nonzero resistance, will cause the wire to dissipate power in the form of heat. Some of the generated heat will likely transfer into the ferrite due to the wire being closely wrapped around the ferrite. Copper wire will increase in resistance when heated, causing the wire to dissipate a greater amount of power in the form of heat. It is obvious that inductors should be used with caution in high current or high temperature conditions. Because the inductance value of the inductor itself is variant with time and temperature, the inductors could be spaced in a different way that will add resilience to the some of the "gaps" in inductance value that can form when the inductors deviate from their ideal value. To illustrate the impact of inductance variation a table is shown below of a worst-case scenario given the manufacturer's specifications.

Table 2: Inductor Tolerances

Ideal inductance (μH)	Tolerance(%)	Resulting Ind. Range (μH)
1	**±30**	**.7-1.3**
2	**±30**	**1.4-2.6**
4	**±20**	**3.2-4.8**
8	**±20**	**6.4-9.6**
16	**±20**	**12.8-19.2**

The tolerances are taken from a Coilcraft datasheet, where the specified inductance tolerances were taken in a temperature range of $-40°$ to 165 ℃ with the current below a specified RMS (root mean squared) value. If the inductance values are uncorrelated and Gaussian in distribution within the specified range, the more inductors

added together to make a specific value, the smaller the variation of the resulting inductance (Gaussian squared, cubed, etc). For example, if 31 μH was made out of the 5 values shown above, the probability that the inductance will be closer to 31 μH will be greater than if a single 31 μH inductor is used with a ±20% tolerance. This is both good and bad, since the theoretical 31μH inductor should be very close to the desired value, but a discrete 32 μH inductor will likely be further away from the ideal value than the 31 μH inductance.

Variation in inductor value will cause the inductance to not steadily increase. Instead, values will be found at which the difference in two neighboring values is greater and less than 1 μH, a similar concept to differential nonlinearities in data converters. In reality, the inductors will be sharing common environmental factors such as heat and current throughput, which will cause the inductance errors to be greatly correlated, which means the inductances are more likely to have a common error. For instance, if the environment to the inductors exhibits a ambient high temperature, the value of each inductor may be lower than the ideal value. The microprocessor will open and close the switches for a given inductance, and the actual inductance will be a lower value than expected. One method to overcome this sort of error is to only require the microprocessor or control system to decide if more or less inductance is needed instead of a specific value. If the actual inductance is lower or higher than expected at a specific value, the microprocessor simply needs to decide if more or less inductance is needed to make the necessary corrections. The control system mentioned earlier can accommodate these types of decisions due to the fact that the microprocessor is receiving a phase measurement from the circuit and deciding using an integrator feedback control system whether the inductance needs to increase or decrease based on a given error term. The actual inductance value is never introduced in any calculations with this type of system, therefore making the system insensitive to inductance *offset* but still sensitive to non-monotonically spaced inductances.

Figure 26 illustrates the inductor values that can be created from a 2^N inductor spacing where N is an integer number. In this example the maximum value of N will be

5, giving a possibility of 31 inductor values from 1 to 31 μH with a 1 μH spacing. Note that the figure below assumes ideal inductor values, i.e. no error.

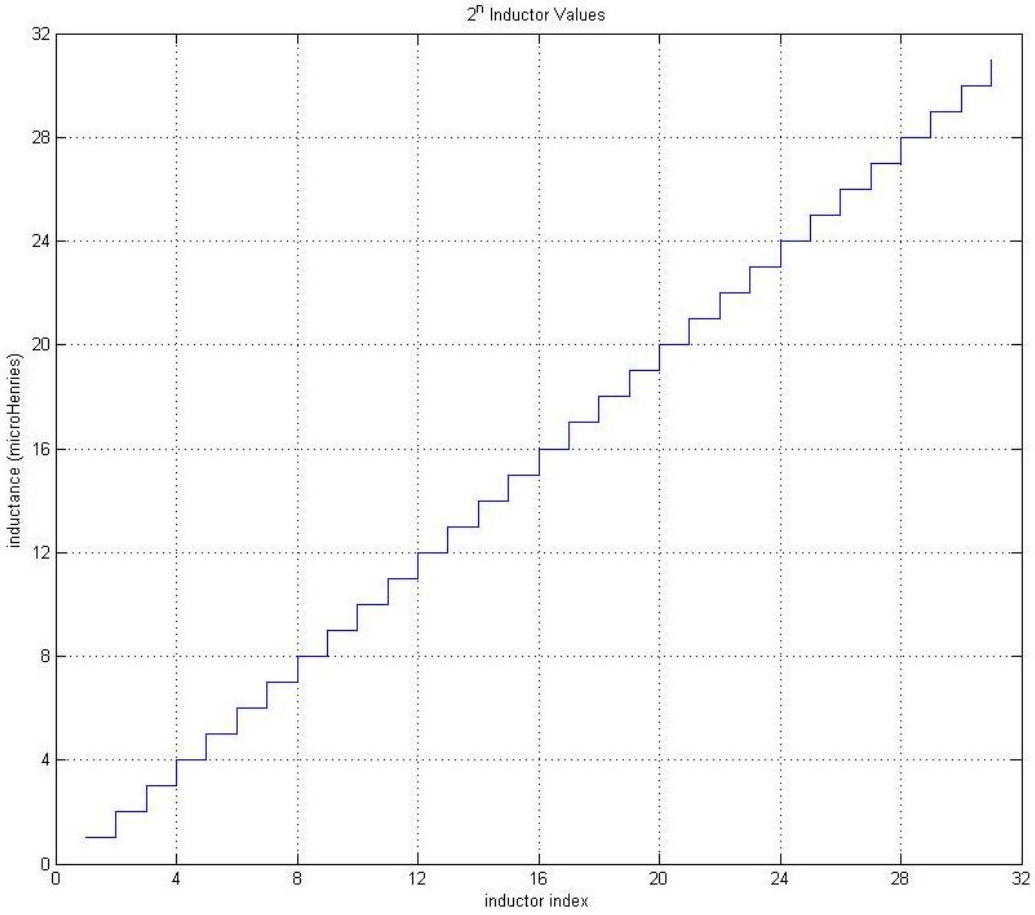


Figure 26: 2^N Ideal Inductances

Because the inductors in this example have a maximum tolerance of ±30%, a smaller value than a power of 2 will be chosen. If the inductors are spaced, by 1.7^N for example, the convenient straight binary property is no longer available. For a given inductance value, the nearest value will be made up with a very different combination of inductors which will distribute the error more evenly as the inductance values increase. This can help minimize the aggregate errors that build up as more inductors are used for each value as the values increase and may lead to more monotonically increasing inductance values. Below is a plot of the 1.7^N spaced inductors. Notice they are no longer sorted in order, which is where the benefit of the design is derived. The next inductance

value in the index, if indexed in the same manner as the 2^N design, may be more or less than the current value.

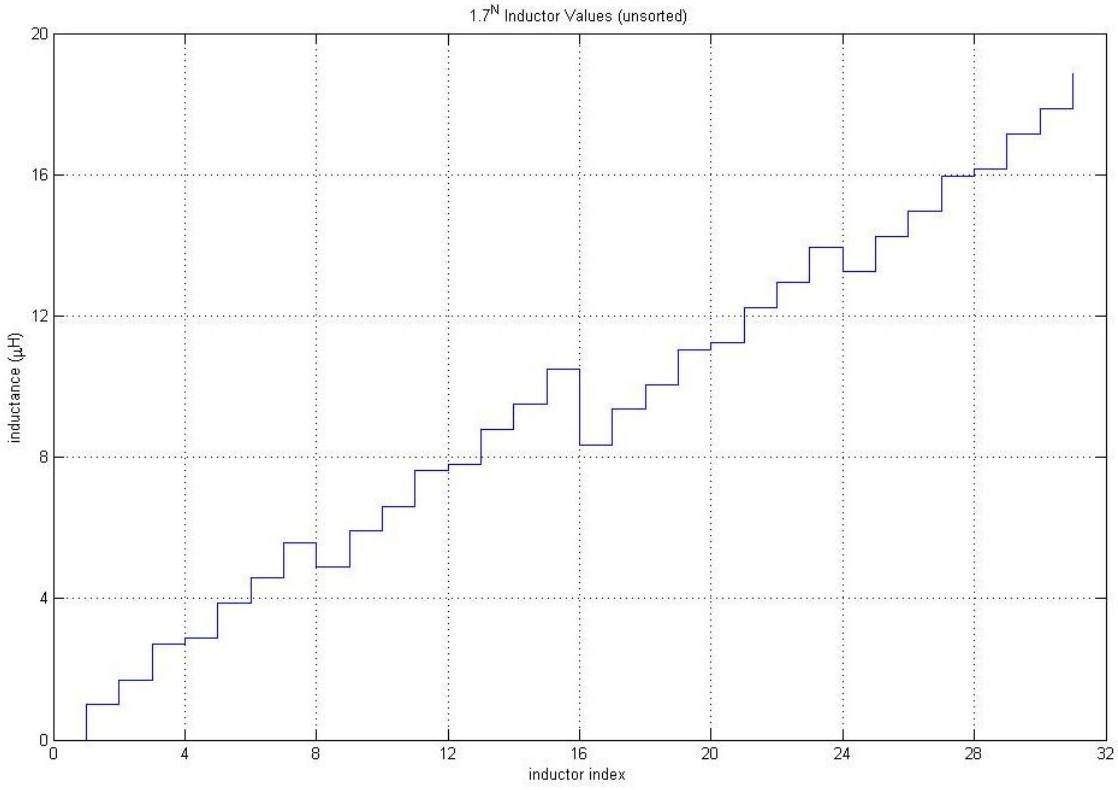


Figure 27: 1.7^N Ideal Inductances

If the 1.7^N spaced inductances are sorted to be in order, the result is a nearly linearly increasing relationship between index and inductance. In Figure 28, the sorted 1.7^N values are plotted along with the 2^N values for comparison. Notice the great decrease in inductance range the 1.7^N design has; this is a significant drawback. Because the inductors are spaced closer together, the range of possible values is greatly reduced for a given number of inductors. By reducing the space between inductor values, a tradeoff has been made. The 1.7^N spaced design is more robust than the 2^N design when inductor value variation is introduced, but has a much smaller range with the same number of inductors.

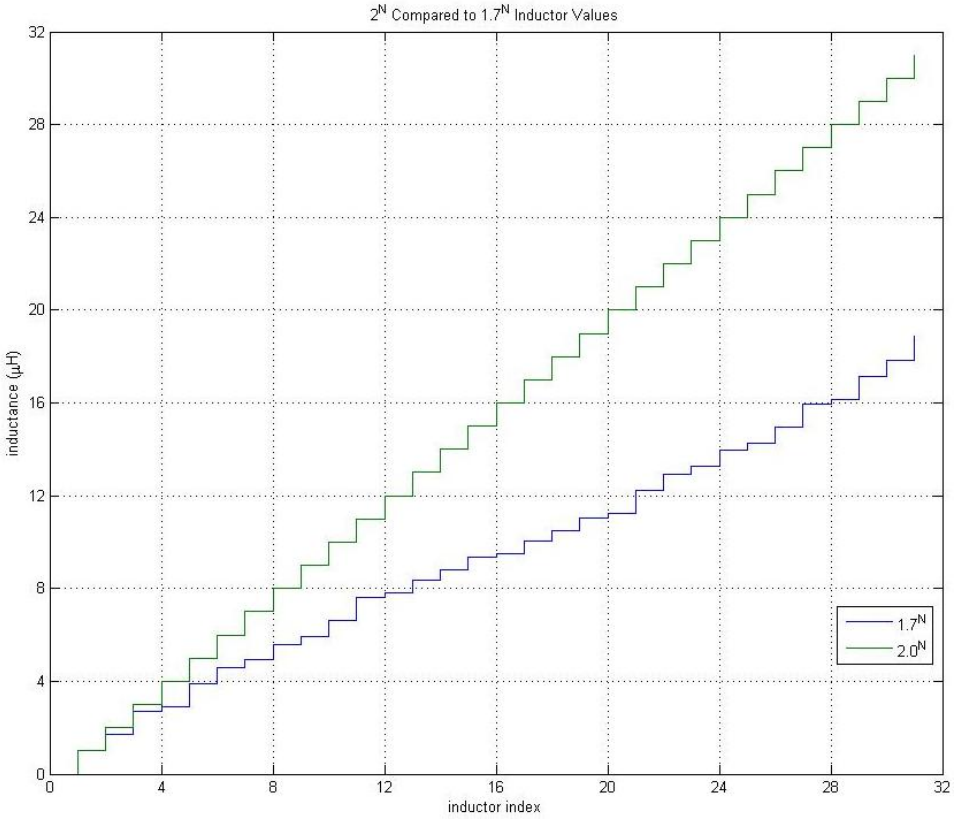


Figure 28: Sorted 1.7^N compared with 2^N Spacing

The inductors themselves, for a space-efficient product, will be mounted on a printed circuit board (PCB) and will be laid out in a compact arrangement. To prevent magnetic coupling due to the devices being in a high density arrangement, a shielded inductor will be chosen. Also, in attempt to alleviate inductance variation, an inductor must be chosen with a tolerance specification that covers a wide temperature range and RMS current rating. Both of these specifications must exceed the expected values in the application. The MSS1260T inductor series made by Coilcraft was chosen because it matches all of the requirements mentioned. The device's datasheet states that the inductors are "Designed for high ambient temperatures", have a "very low DCR" (DC resistance), "excellent current handling" and "magnetic shielding allows high density mounting" (Coilcraft). The inductors come in an SMT (surface mount) package that allows for efficient assembly and a space efficient hardware design.

The switches used to insert and remove each inductor from the series circuit must be controllable by a microprocessor. These switches must also be capable of handling and breaking the required currents. Relays provide the favorable current handling and breaking characteristics but require a large amount of current to activate; too much for a small microprocessor's IO (input output) pins to drive directly. Because there will be two variable inductors included in the design, there will be a large number of relays to control. Because small, low-cost microprocessors usually do not have a high IO pin count, an external device must be used to control the bank of relays.

To add inherent flexibility to the design, two inductors will be included at each inductor and switch site. This allows two inductors to be paralleled to achieve a desired value. Because inductors are typically manufactured in less than useful values, two inductors can be paralleled to create almost any desired value. In addition to gaining more control over inductance value, two inductors in parallel also reduces the current flowing through each, potentially relieving some of the inductance variation due to current throughput and heating. Also, because more inductors are used to make a given value, the variations in each discrete component may sum to a value closer to the desired inductance than if fewer inductors were used. If two inductors are to be used, the current loading in the relay can also be reduced by using a DPDT (double-pole double-throw) relay. If one inductor is connected to each switch in the relay, the contacts in each switch will have to handle and break less current than if both inductors were electrically connected to the same contact. Figure 29 illustrates these concepts.

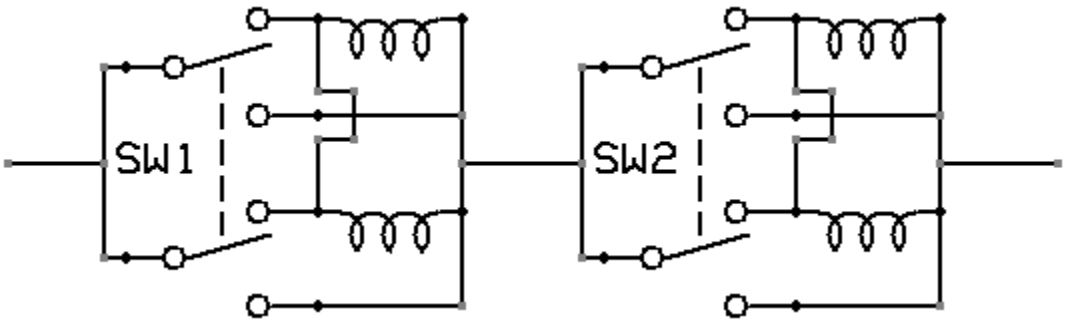


Figure 29: DPDT Relay and Parallel Inductors

The switches in Figure 29 represent the internal circuit of a relay. The poles are both controlled by the same control signal and do not operate independently. In one switch position, current is passed from the input node, through the two inductors and on to the next switch-inductor combination. In the other switch position, current bypasses the two inductors, effectively eliminating them from the series circuit, the same concept as the SPST (single-pole single-throw) switch circuit discussed in Figure 24 and Figure 25.

Another important consideration is that combining switches and inductors can potentially create large and potentially damaging voltage transients. The voltage across an inductor is equal to the inductance multiplied by the derivative of the current with respect to time. When the derivative of the current is very positive or very negative the voltage across the inductor will be very large. High current derivatives can easily be created with switches making and breaking the current path with an inductor. The largest voltage transients will occur when the switch is transitioning between contacts, when both terminals of the inductor will be floating. When the switch has been thrown, it will transition from one pole to the other and will bounce on and off of the contact of the destination pole. This bouncing action will rapidly make and break the current path with the inductor. To protect other circuit elements from high voltage transients, a clamping device can be used to limit the voltage range allowed on a given circuit node. This is easily done with two opposing Zener diodes. When the voltage across a Zener diode reaches a specific voltage called the Zener voltage, the diode breaks down and acts like as short circuit. If two Zener diodes share a common anode, the two cathodes can be placed across a device. If the voltage across the device exceeds the Zener voltage in the positive or negative direction, the reverse biased diode breaks down and conducts through the already conducting diode. This configuration will "clamp" the voltage inside the range specified by the Zener voltage of the two diodes. To clamp the voltage across each inductor, the two Zener diodes will be placed across each inductor and switch group. A Zener voltage of 120 V has been chosen to maintain a maximum allowable voltage at

these nodes. The Zener voltage was chosen to be much higher than the expected normal voltage range so that the diodes do not start to break down during normal conditions.

Another important topic that must be addressed is the means by which the microprocessor controls the relays. Most low-cost microprocessors lack the number of pins to control each relay independently. In the case of having too few IO pins, device called a "port expander" is appropriate. The particular device, the MAX7301, has a serial port over which it can receive commands from a microprocessor. The MAX7301 has 20 user definable IO pins that can be controlled through the serial port. This reduces the size and cost of the microprocessor and provides all of the necessary control required for both of the variable inductors (up to 20 relays). The MAX7301, however, does not have the current driving capacity to drive the relays that were chosen to switch the inductors in and out of circuit. The AXICOM relays that were chosen require 30 mA of sustained current to stay switched. Electrically, the internals of the relay control circuit are very inductive in nature. To avoid damage to the MAX7301, a buffer driver can be used that has built-in Zener protection diodes. The NUD3105D, made by ON Semiconductors, is called an "Integrated Relay, Inductive Load Driver" and is capable of driving relay coils rated up to 2.5 W at 5 V and contains all of the necessary Zener clamping diodes for protection. The NUD3105D device will drive the relay coils used in switching inductors in and out of circuit. To signal the NUD3105D devices, the MAX7301 IO expander will be used, which will be controlled by a microprocessor through a serial port.

The range of inductance values has been determined based on the specified frequency range and the electrical properties of the transducer being used. The variable inductor will be able to range in value between 0 and 127 μH with steps of .25 μH, requiring 9 inductor-relay sets. Two additional relays have been included for added flexibility. One relay is able to open-circuit the parallel inductor if no parallel inductance is desired and the other is able to switch the position of the parallel inductor to be directly in parallel with the load. This feature increases the range of load impedances that can be matched. In Figure 30, a circuit diagram illustrates all of the concepts that were discussed regarding the variable inductor design. The measurement circuitry, relay drivers and

microprocessor are all excluded from this diagram for clarity. These elements can be viewed in Figure 42 and Figure 43.

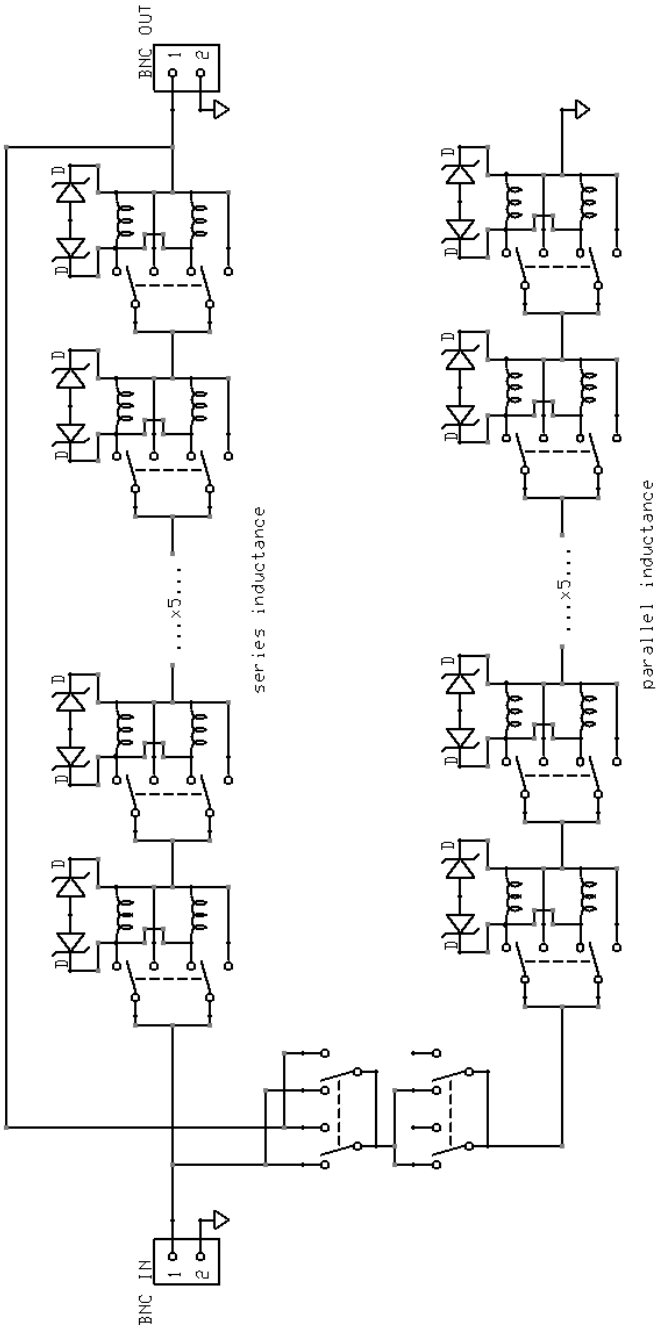


Figure 30: Series and Parallel Variable Inductor Circuit

3.3 Variable Inductor Testing

To test the variable inductor design, the series inductance will be swept from 0 to 63 µH, just like the scenario in Figure 17 and Figure 18, and compared to the ideal calculated value. The test scenario was taken at 700 kHz using a 30 Ω resistive and 1.5 nF capacitive load. The figure below displays the results of 5 separate tests to verify the consistency of the measurements.

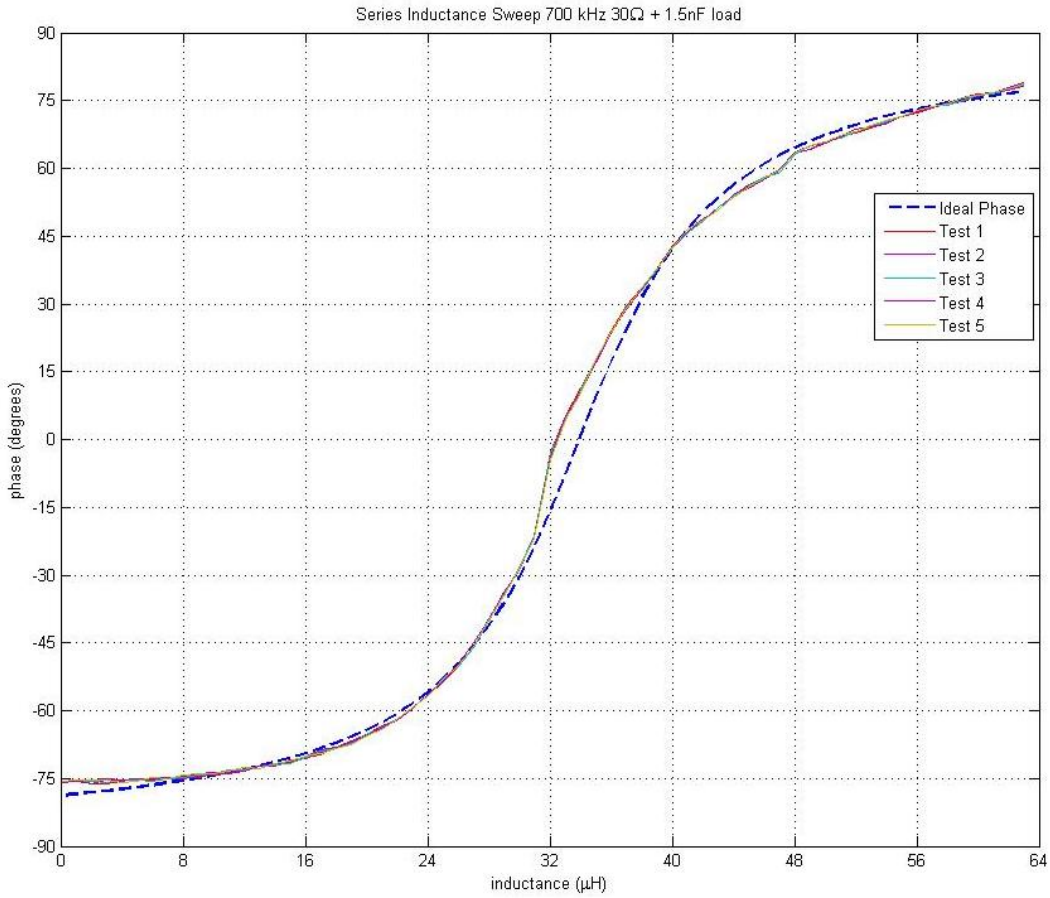


Figure 31: Measured Phase Angle

The ideal calculated result is indicated as the bold dashed blue line. The measurements were taken from the phase detection circuit itself and logged via serial link to a computer, thus representing a completely hardware based measurement. If this data is taken and combined with the measured voltage and phase data, the measured resistance and reactance can be extracted and analyzed. The deviation of phase value between

sweeps is very small, indicating a measurement circuit that is capable of producing very repeatable measurements.

The measured reactance of the test load including the series inductance is shown in Figure 32. The measured reactance in bold green has been assigned a linear best-fit curve. The data in red indicates the difference between the measured curve and the best-fit linear approximation. This data can be used to determine the linearity of the measured reactance. Ideally the reactance should linearly increase as the inductance is being linearly swept from 0 to 63 µH. This test requires the calculation of reactance, which requires Zmag and phase to be measured. The calculation of Zmag requires Imag and Vmag to be measured. Because calculating the reactance requires several measurements, some error may be introduced by inaccuracies in each.

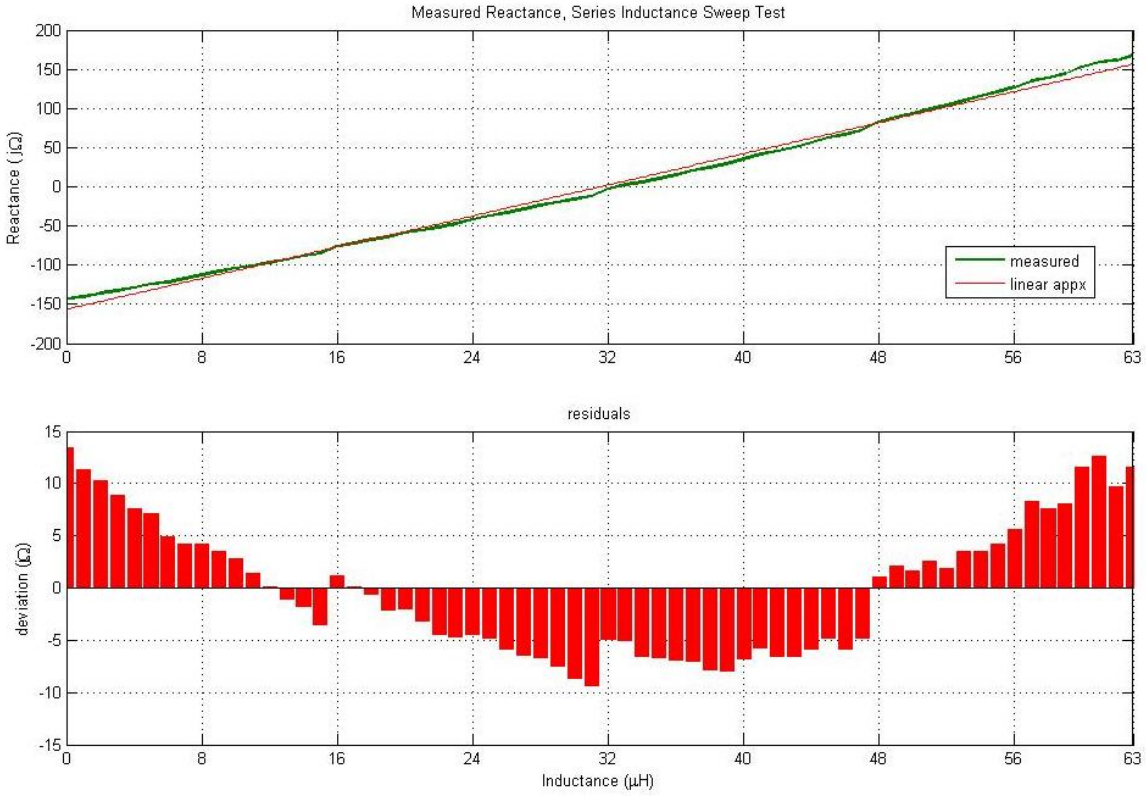


Figure 32: Measured Reactance of Test Load

To get an idea of system performance with the actual ultrasound transducer as its load, the same inductance sweep test is executed at different frequencies. The results of this test are displayed in Figure 33 and **Error! Reference source not found.**. This test reveals some interesting information about the frequency response of the transducer. The rate at which the phase changes is not constant with frequency. Some of the phase transitions are quite sharp and others are much more gradual. The sharp transitions indicate that the real resistance at the particular frequency is smaller than at the frequencies that show a gradual phase transition. It can also be seen that the point at which the phase passes through zero is not directly dependant on frequency. Notice that at 375 kHz, the phase passes through zero at around 50 μH, at 395 kHz 46 μH and at 415 kHz the inductance that produces zero degrees in phase jumps over to 32 μH and then *increases* back to 37 μH at 435 kHz. This indicates that the reactive element, in this case the capacitive term in the transducer, is not changing linearly with frequency. From this test, it can be concluded that neither the real or imaginary part of the load impedance is constant nor consistently increases or decreases with frequency.

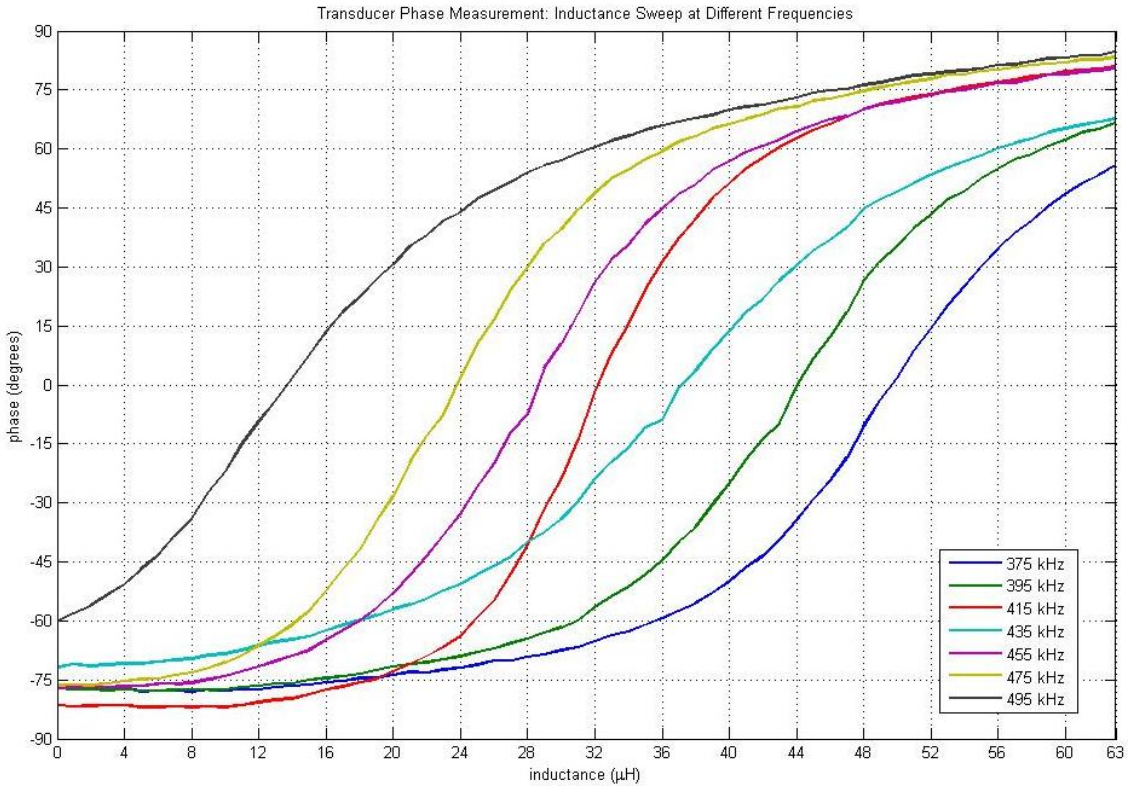


Figure 33: Phase Measurement of Transducer, Varying Frequencies

Table 3: Series Inductances that Cancel Transducer Reactance

Frequency (kHz)	Ltune (µH)
375	50
395	45
415	33
435	38
455	30
475	25
495	15

The methods and subjects that have been discussed in this chapter provide a foundation for maximizing power transfer into a resistive and reactive load. Next, hardware must be created that utilizes these concepts.

Chapter 4

Hardware, Implementation and Results

Now that the methods for completing the requirements for maximum power transfer have been introduced and some testing data has been presented, a working hardware design must be implemented. The hardware design process in this project, so far has spanned 3 revisions. The first hardware revision was created to be a prove the design concepts that have been established. Each succeeding revision adds features or corrects problems found in the previous revision. Revision 3, the final revision, is able to maximize the power transfer into the ultrasound transducer using the feedback techniques discussed in previous chapters. This chapter will illustrate the design process and display some final testing results of revision 3.

4.1 Hardware Revision 1

Revision 1 was created to be a testing platform for different measurement methods. Voltage, current and phase are measured in many different configurations to determine which method yields the best results in hardware. Revision 1 also proves that a low cost microcontroller is able to convert analog measurements into impedance information. In addition to impedance measurement, in this design, the microcontroller performs very accurate frequency measurement, allowing direct calculation of the resistance, inductance and capacitance of a load. Some unforeseen problems that were brought forth in this design involve power supply design. A large portion of the design's complexity involves the power supply circuit. A total of 5 power rails are used, which occupy a large amount of circuit board space and use a large number of parts. This revision emphasized the importance of simple power supply in a hardware design, a concept that is taken into consideration in future revisions.

The microcontroller used in revision 1 is the MSP430F2274. This low cost microcontroller features a moderate pin count, a single hardware UART serial port and a 10-bit ADC. This particular family of microcontrollers is known for extremely low power consumption when operating in special low power modes. The low power mode feature

makes the MSP430 series highly suitable for battery powered devices. Because this application does not require any such features, the MSP430 microcontroller was chosen for its personal familiarity and features other than low power operation.

Other features in revision 1 include a USB serial port for data logging, and a text LCD screen for monitoring impedance and frequency information. Revision 1 is considered a success. This revision provided all of the required design insight for future revisions, including proof that impedance can be measured using analog circuits and a low cost microcontroller. Figure 34 displays the top layer of the revision 1 PCB.

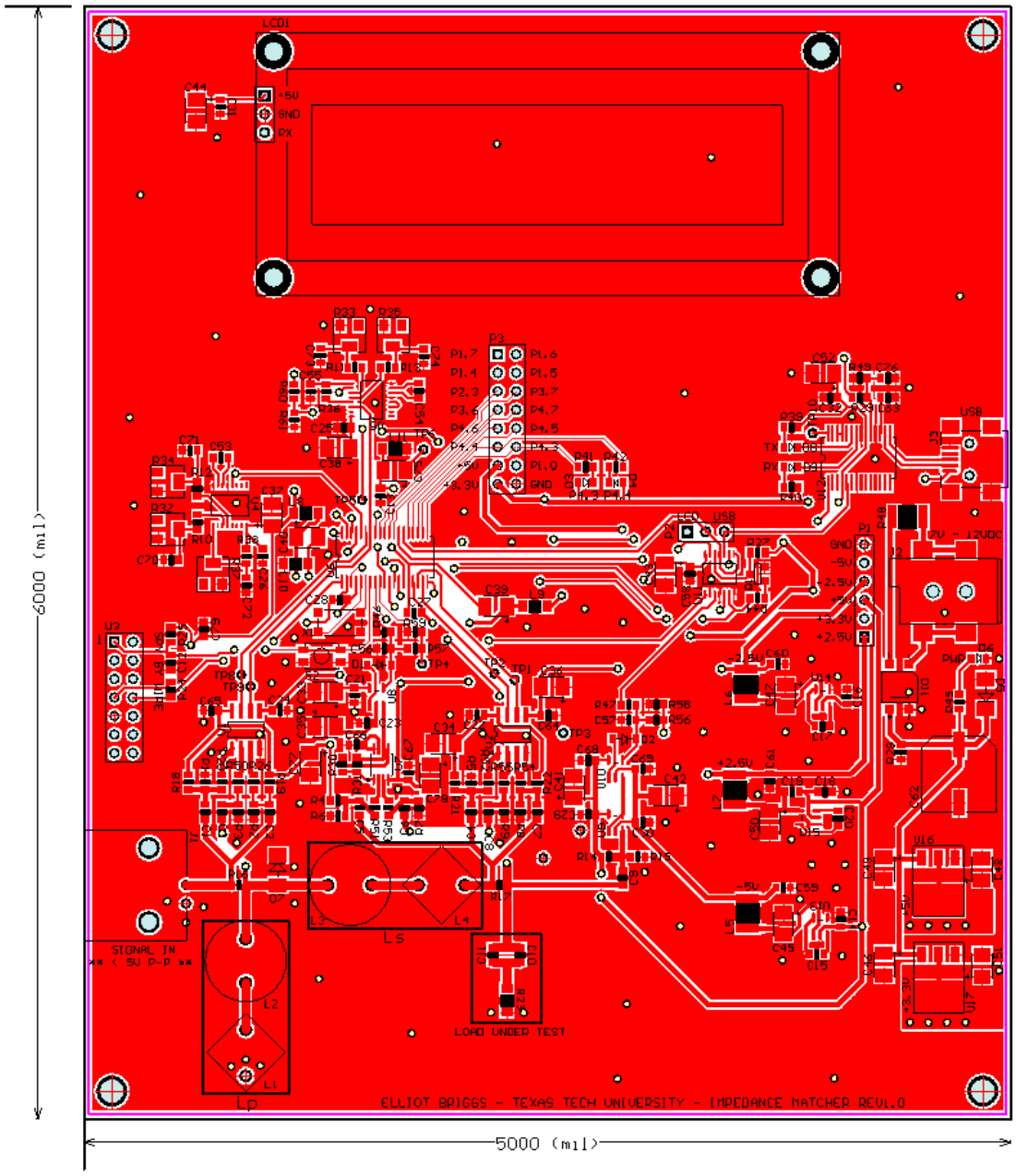


Figure 34: REV1 PCB Top Layer

4.2 Hardware Revision 2

Revision 1 does not feature a variable inductor or any other method that can be used to cancel reactance or match impedance. Revision 1 simply takes measurements and reports them to the user. Revision 2 includes two variable inductors that can be manipulated by the user, as well as by automatic control. Because the successful measurement techniques from revision 1 were translated into revision 2, a control system that automatically matches the source and the load impedance can now be designed.

A design goal for revision 2 was to create a user friendly hardware form-factor. The circuit boards are designed to be mounted inside of a vented two unit (2U) rack-mount enclosure. The signal generators that are being used are rack mountable, so by making the impedance matching devices rack mountable, portability of the entire system can be increased. If every component of the system is mounted on a single rack, moving the system to another lab is more convenient. Another design feature that was added to enhance user friendliness and compatibility is the integration of a universal power supply. The power supply that was chosen for revision 2 can accept 110-220VAC at frequencies of 50-60 Hz and is fitted with a universal power socket that allows the device to be connected to any power outlet type (UK, continental Europe, USA, etc.). The power supply is also UL approved which may help if the system is required to go through the UL approval process.

Updates to the digital portion of the design from revision 1 include a more powerful microcontroller, the MSP430F249, which has 2 hardware UARTs, a 12-bit ADC, and more general purpose input-output (GPIO) pins. The two hardware UARTs are used to communicate with the LCD module, the USB interface as well as an optional Bluetooth modem. The Bluetooth and USB share a UART port through a 2 x 2:1 multiplexer.

The overall design of revision 2 is split into two circuit boards. One board contains the power supply and digital devices, while the other contains the variable inductor and analog portion of the design. The design was split to allow updates or a

redesign of the "inductor and analog" board without having to redesign the "digital and power" board. The two boards are connected by a large pin-count connector that contains both power and signal nets.

To control the inductors, a LabVIEW graphical user interface (GUI) was created. With the LabVIEW GUI, the user can control the inductors and log measurement data on a PC. The serial communication with the PC is done via the USB or Bluetooth interface. All control commands issued by the GUI are send through the serial link and interpreted by the MSP430.

A majority of the problems with revision 2 are related to signal integrity. Both of the circuit boards were fabricated using only 2 copper layers, making proper routing of power and signal nets very difficult. Because only two copper layers are present, all power and signal nets are routed using traces. Proper design places power and ground nets as large copper planes. Most of the signal integrity problems are caused by high current power nets routed as traces rather than planes. Copper traces, especially thin ones, have a high value of inductance and resistance. If power is supplied through a copper trace with high inductance, any abrupt change in current through the trace will induce a large voltage transient. Digital devices are especially notorious for abruptly changing their supply current levels. When a digital device switches the value of a signal from a logic high to a logic low, the digital device charges or discharges capacitances, greatly increasing or decreasing the amount of current the device consumes. These abrupt changes in current, combined with the high inductance copper traces, cause the power and ground nets to be tainted with switching transients. If the power and ground nets are not properly designed, digital switching transients will contaminate signals throughout the entire circuit. This becomes a very problematic when sensitive analog measurements are being made on the same circuit board as switching digital circuits.

It is possible to design a circuit that contains both analog and digital devices, as long as care is taken in the circuit board design to assure proper routing techniques. To avoid contaminating the analog signals with digital switching transients, a split power

and ground plane can be used. A split plane technique can partitions the transient filled digital power planes the more quiet analog planes. This technique is useful as long as the power and ground planes of each section are joined at a single point near the power supply and do not physically overlap on the circuit board so that the planes do not couple electrically. Because this technique involves routing both power and ground through copper planes, ideally, the planes should not be segmented among themselves. The planes should be very continuous and allow short current paths for power and ground. Because continuous planes are optimal, a multilayer circuit board is essential. By assigning an entire internal copper layer to the power and ground net, signals can be routed on the top and bottom layers in a much more ideal manner. The revision 3 circuit board is designed using a 4 layers to drastically improve signal integrity. The 4 layer board adds extra cost to the design, but improves the signal integrity greatly.

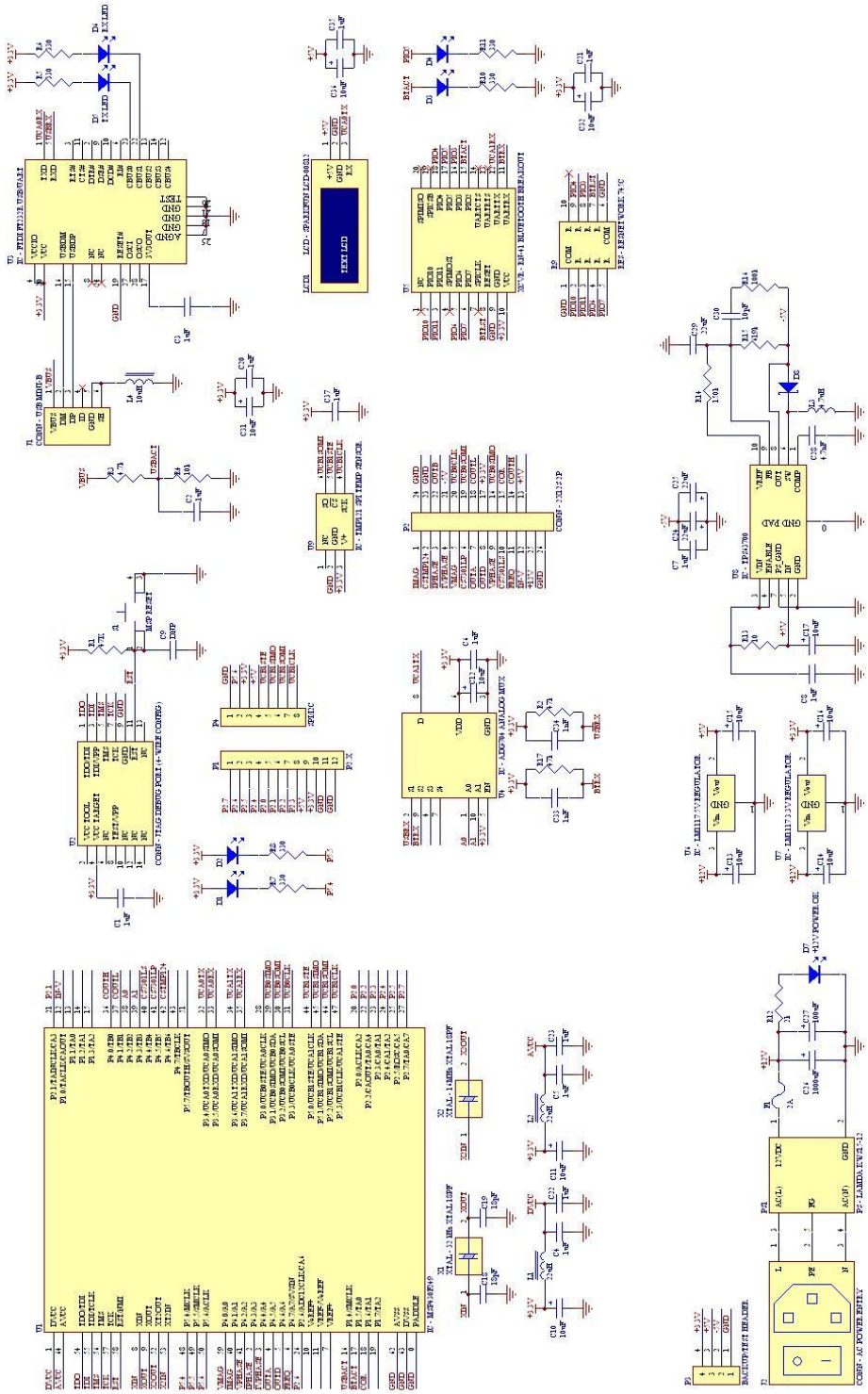


Figure 35: REV2 Power and Digital Board Schematic

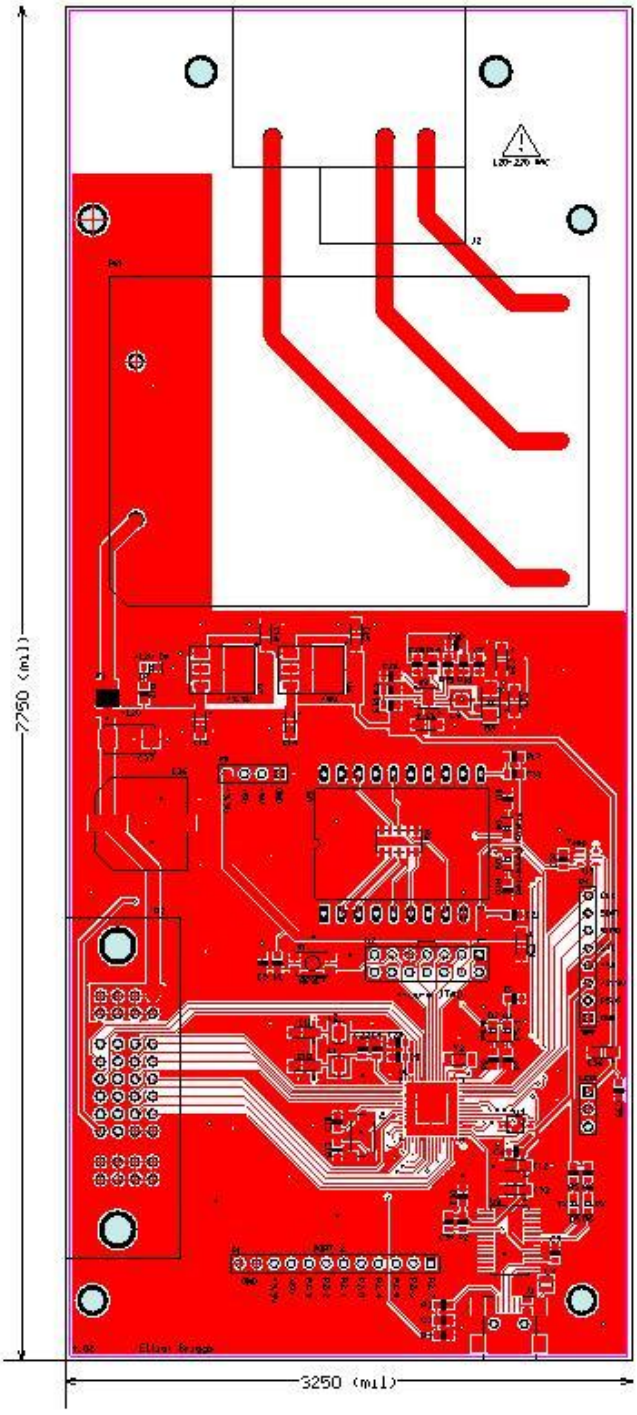


Figure 36: REV2 Digital Control and Power Management PCB

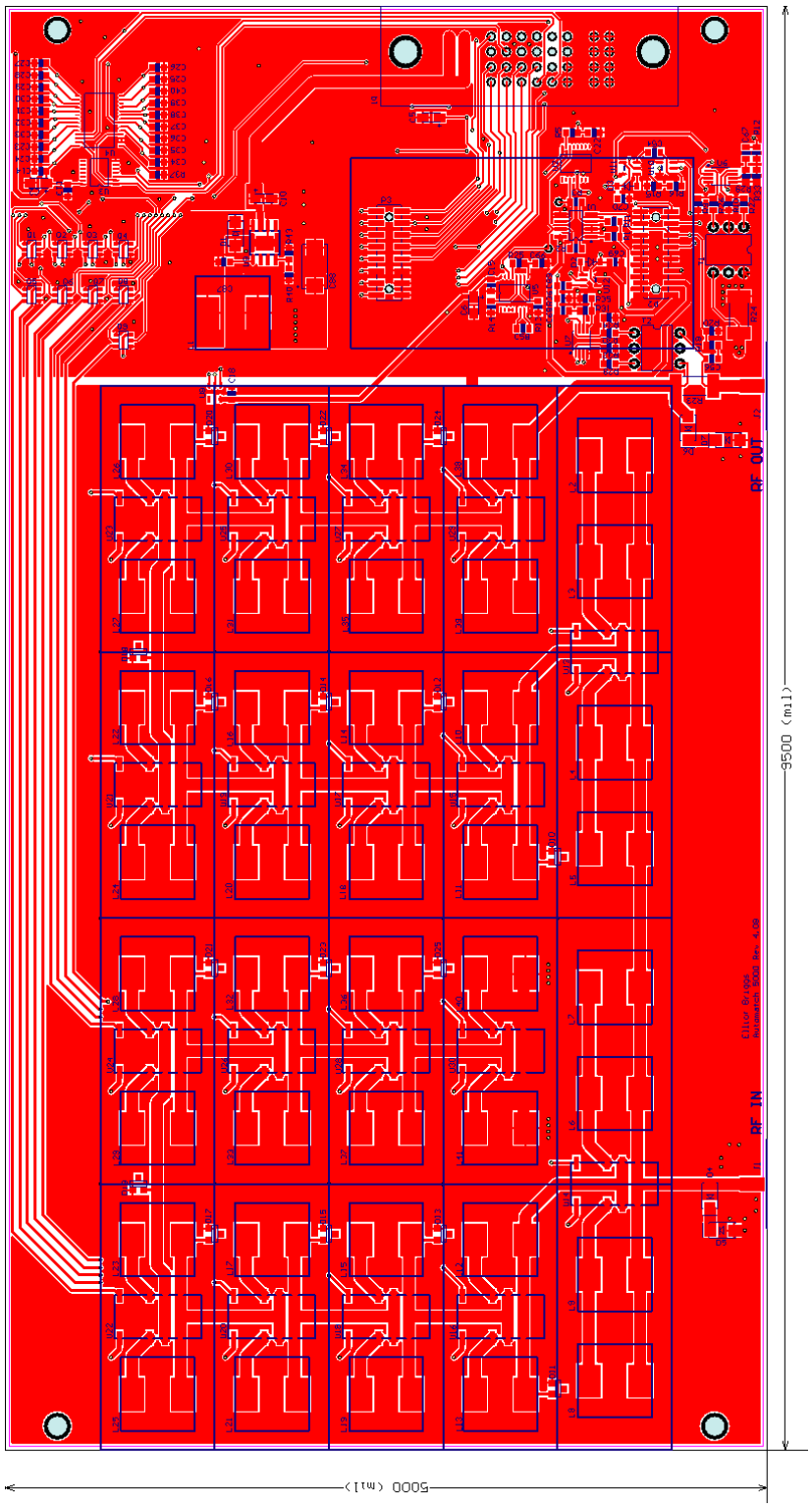


Figure 37: REV2 Variable Inductor and Analog Circuits PCB Top

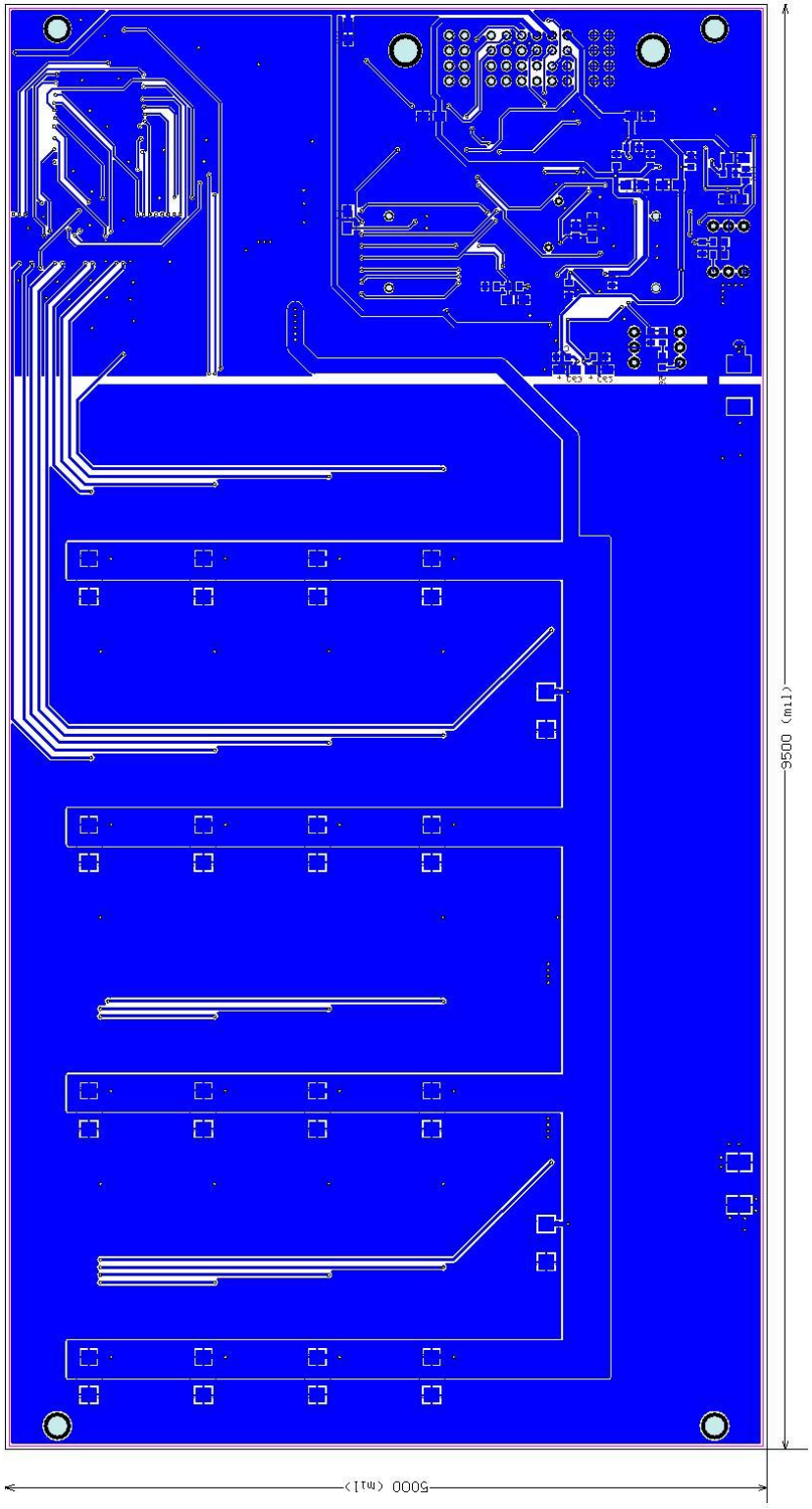


Figure 38: REV2 Variable Inductor and Analog Circuits PCB Bottom

4.3 Hardware Revision 3

The third hardware revision is the final revision that has been built. In this design, the "two board" design was not utilized because the circuit was redesigned on a multilayer board. In addition to being a 4 layer circuit board design, revision 3 utilizes many other methods to improve signal integrity such as placing ferrite beads and a low equivalent series resistance (ESR) decoupling capacitors near device power pins. The signal integrity improvement obtained in revision 3 compared to revision 2 is dramatic.

Revision 3 also features a new power supply design. To save expensive 4 layer board space, bulky power supply circuits were placed on an external and less expensive 2 layer circuit board. Because space on the 2 layer power supply board is less expensive, the power supply circuits can be properly designed with large power and ground planes. The power supply board contains a set of switching regulators that efficiently step the main +12 V power supply into lower voltage rails. Because switching regulators can produce an unwanted level of voltage ripple, a set of linear voltage regulators capable of rejecting ripple are used to further reduce the voltage. The linear voltage regulators are located on the main circuit board which is connected to the power supply board using a cable. The resulting power supply design yields a very "quiet" set of supply rails that are much more efficiently regulated than revision 2. This is made possible by the use of both switching and linear regulators as well as proper circuit board design.

Differences in the variable inductor and the analog circuit design between revision 2 and 3 are minimal. Several additional relays were included in revision 3 that allow the user to eliminate or switch the orientation of the parallel inductor in the matching configuration. An extra feature that has been added to the power supply board is a DC fan controller. A small MSP430 was included in the design to monitor the temperature of a thermistor and can adjust the speed of a DC fan via PWM. The circuit can control two 12 VDC fans to cool the inductors during operation.

Revision 3 has proven to be successful. A feedback control loop that maximizes power transfer has been successfully created. The signal integrity problems that were

present in revision 2 were solved and an optimal power supply design was found. The only known problem is the voltage clamping Zener diode orientation on the variable inductors. The schematic indicates two opposing Zener diodes, one diode has its anode connected to the inductor and the other diode has its anode connected to ground. The correct orientation of the diodes should have the same two common cathode Zener diodes, but with the anodes connected to either side of the inductor that is being protected. The diodes are intended to clamp the voltage across the inductor.

Future plans for this revision include the creation of a user interface console. A header has been included on the revision 3 circuit board for this purpose. An external circuit connected to this header can allow the user to interact with the device using buttons, knobs, and switches. Currently all input from the user is done through serial commands from a computer.

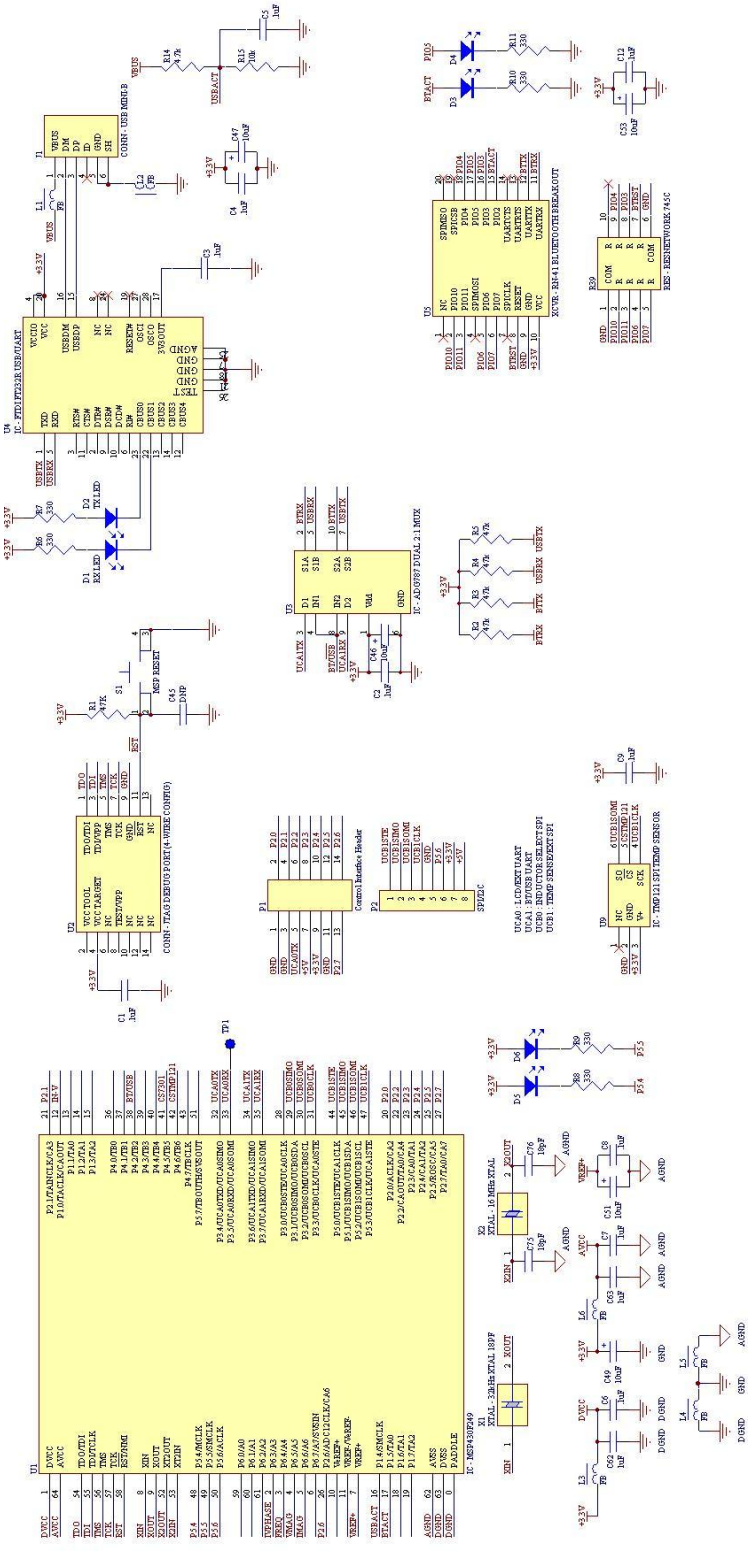


Figure 39: REV3 Schematic Digital Section

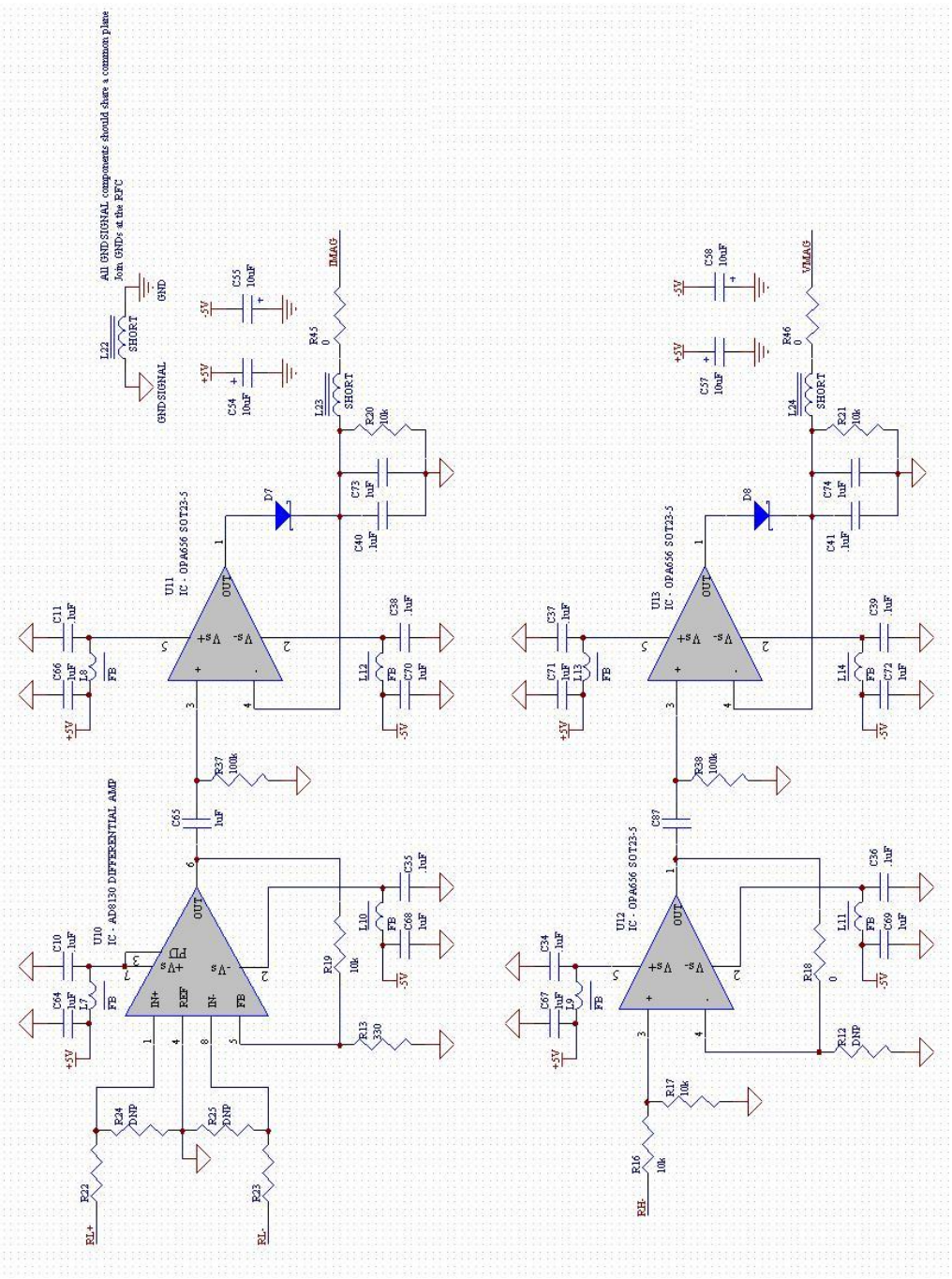


Figure 40: REV3 Imag and Vmag Measurement Section

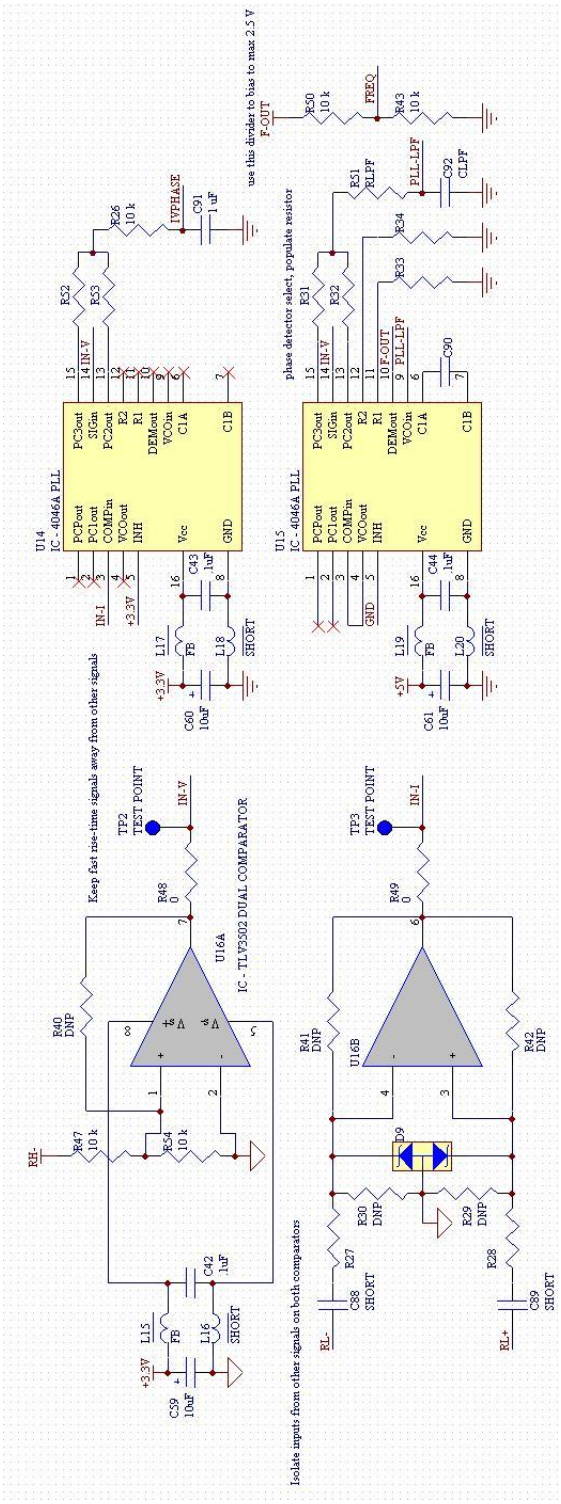


Figure 41: REV3 Phase Measurement Section

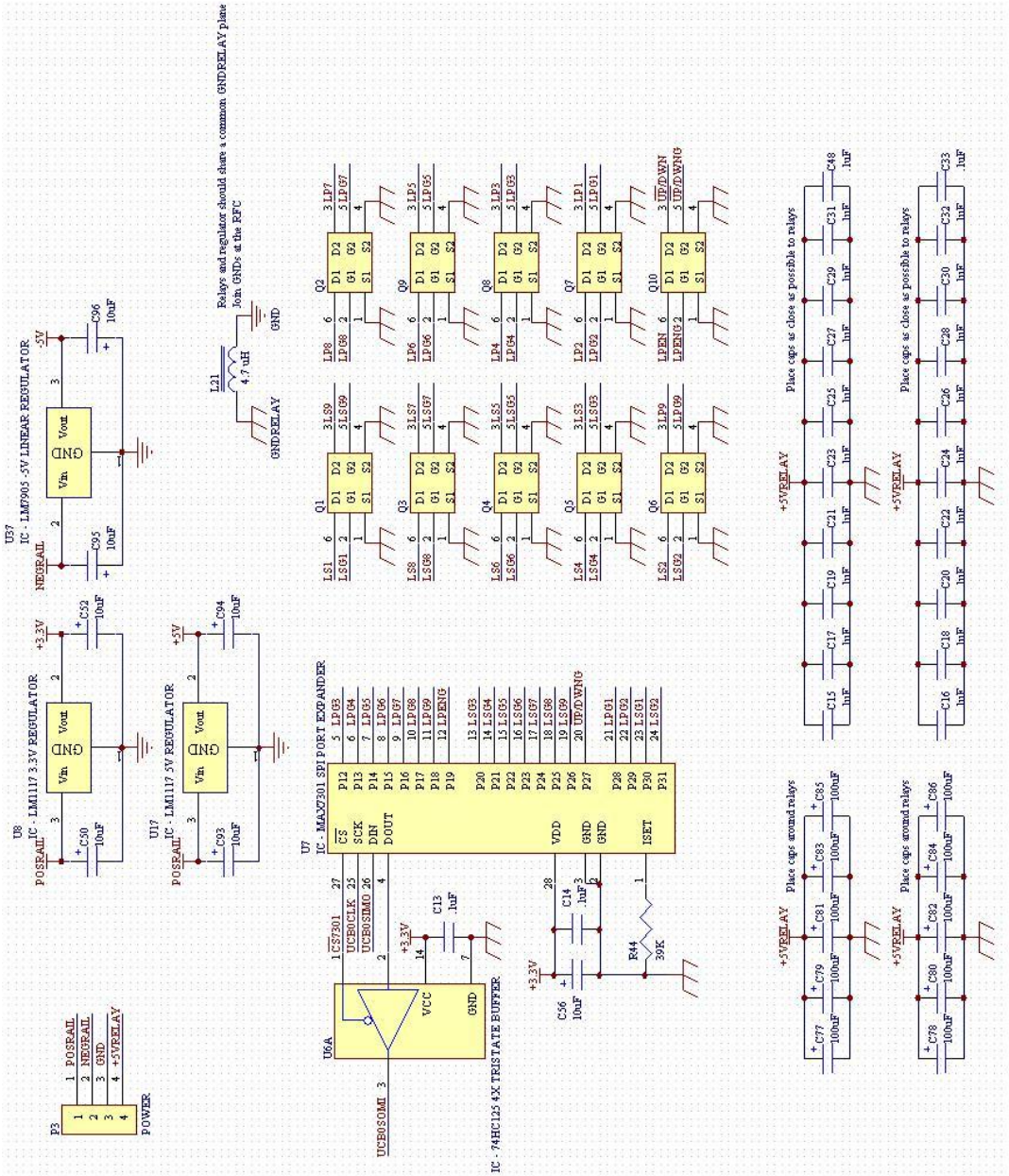


Figure 42: REV3 Relay Control and Driving, Power Regulation

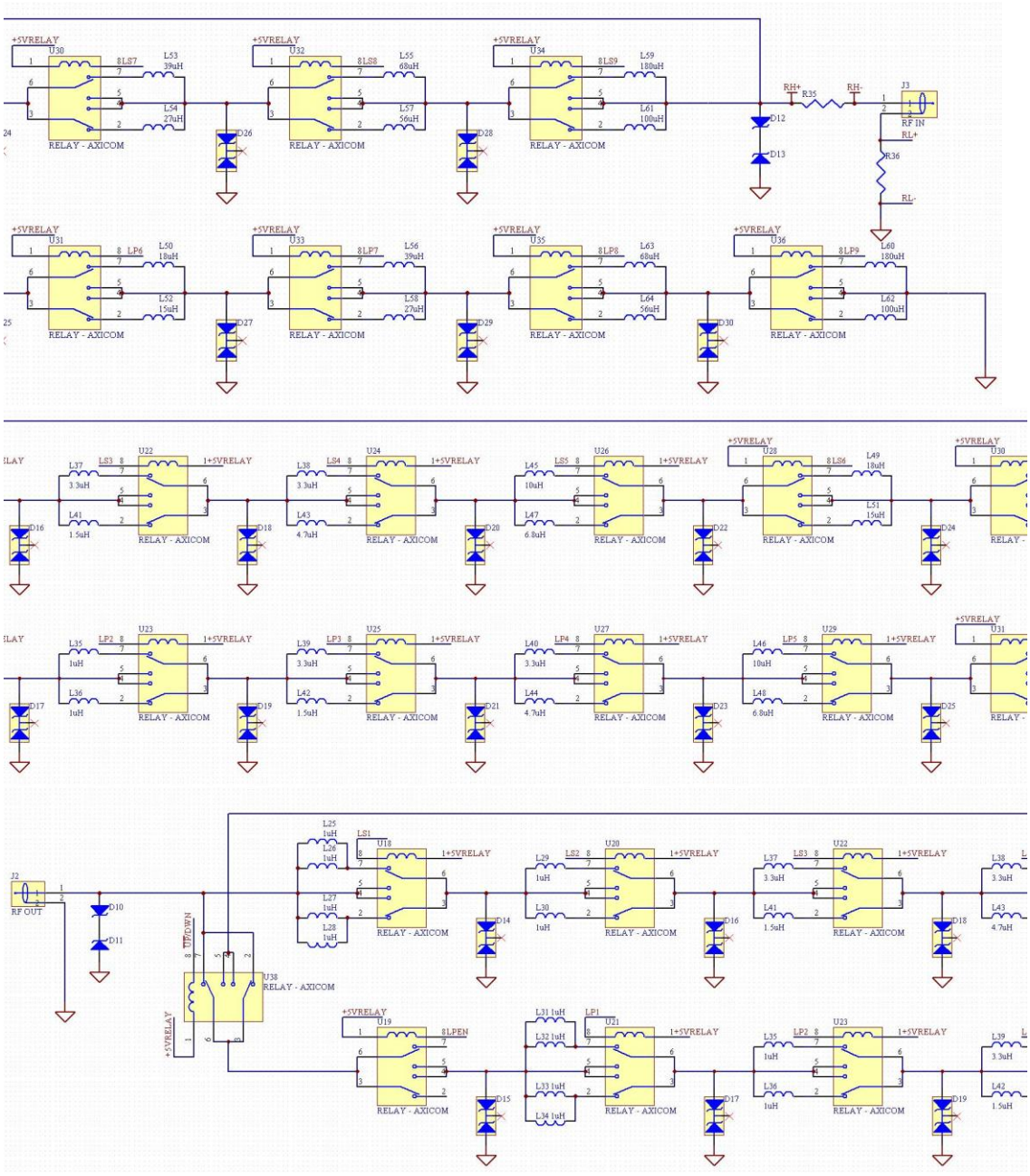


Figure 43: REV3 Variable Inductors, Series and Parallel

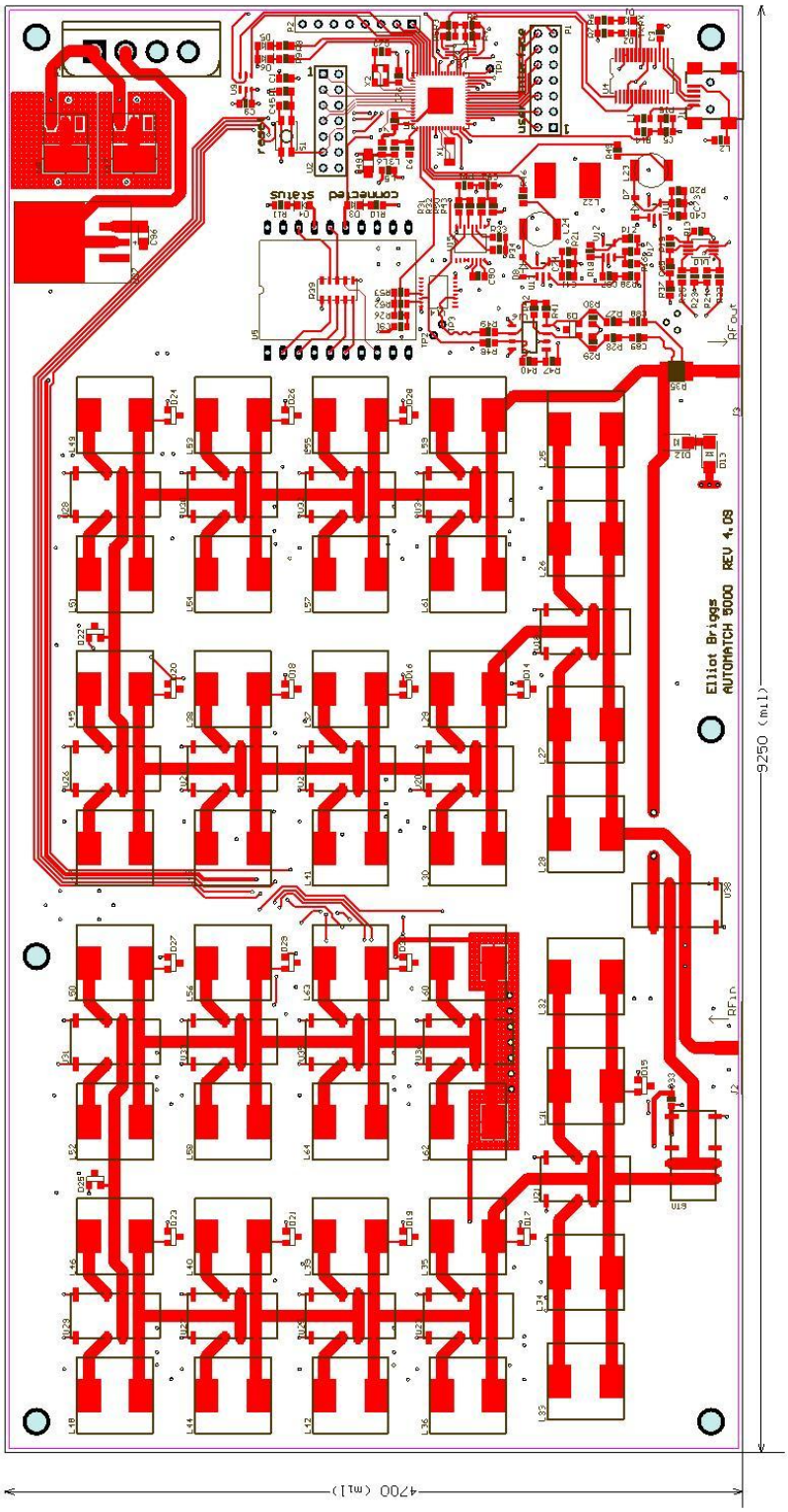


Figure 44: REV3 PCB Layout Top

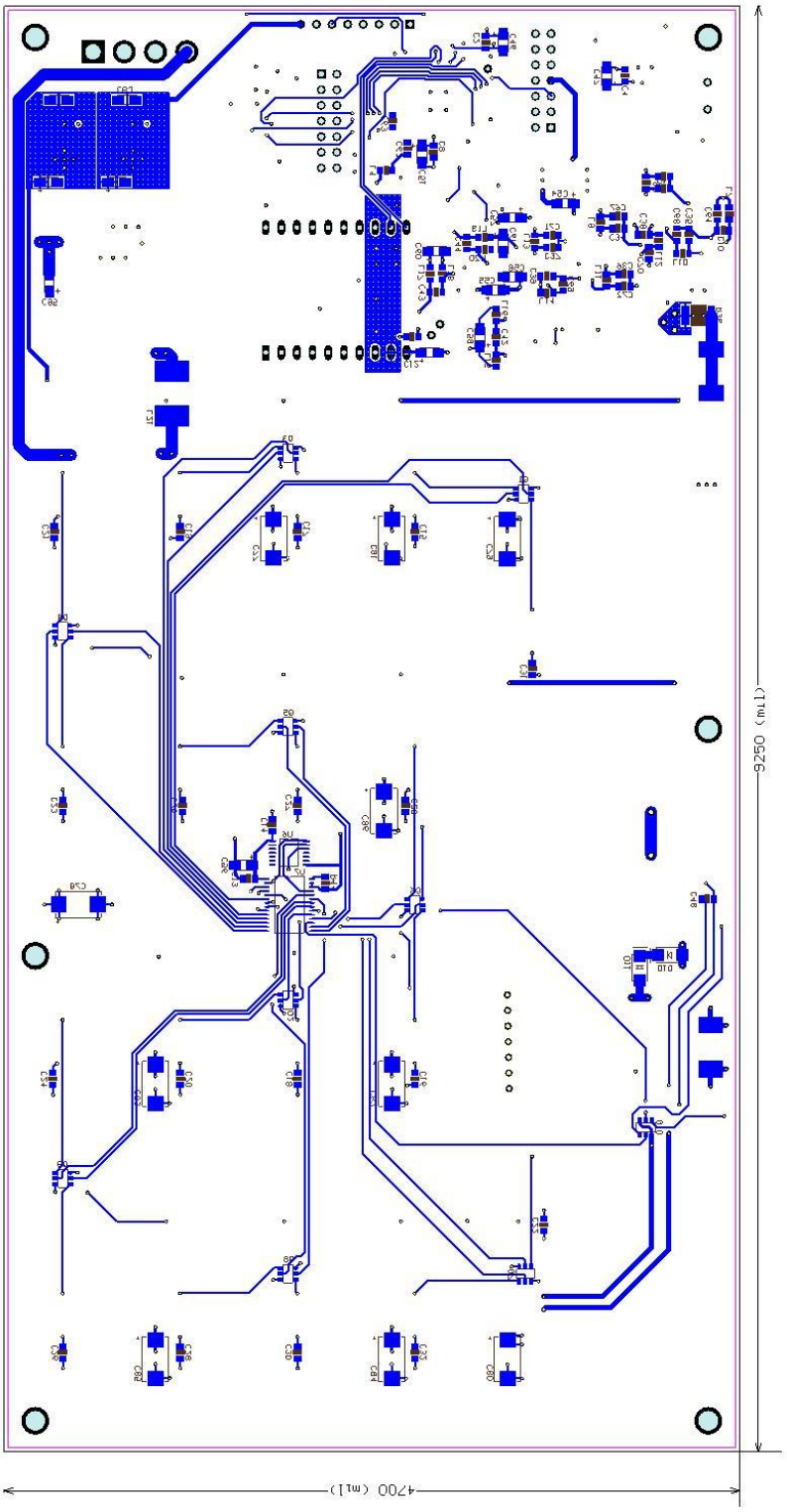


Figure 45: REV3 PCB Layout Bottom

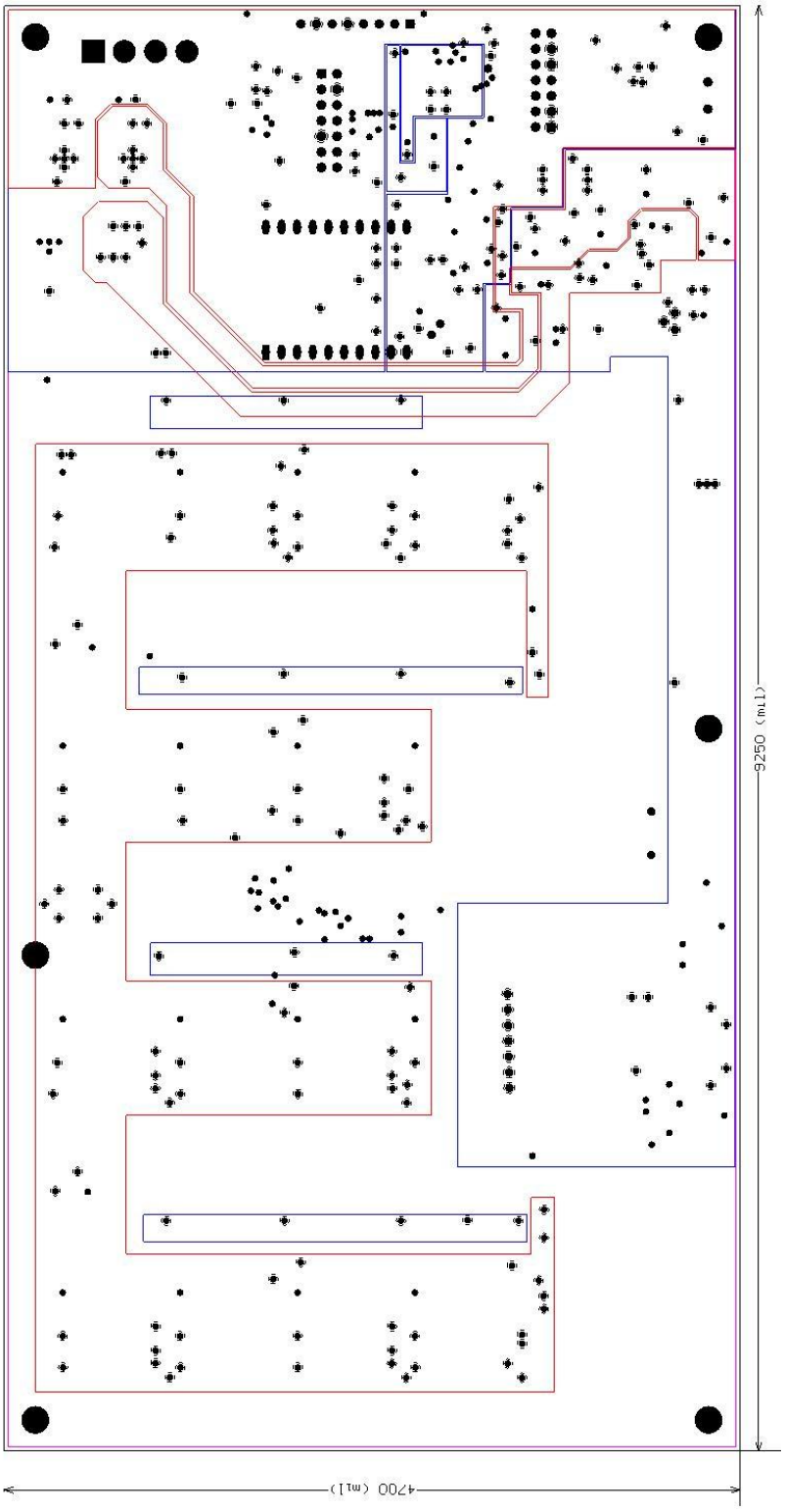


Figure 46: REV3 PCB Internal Layers

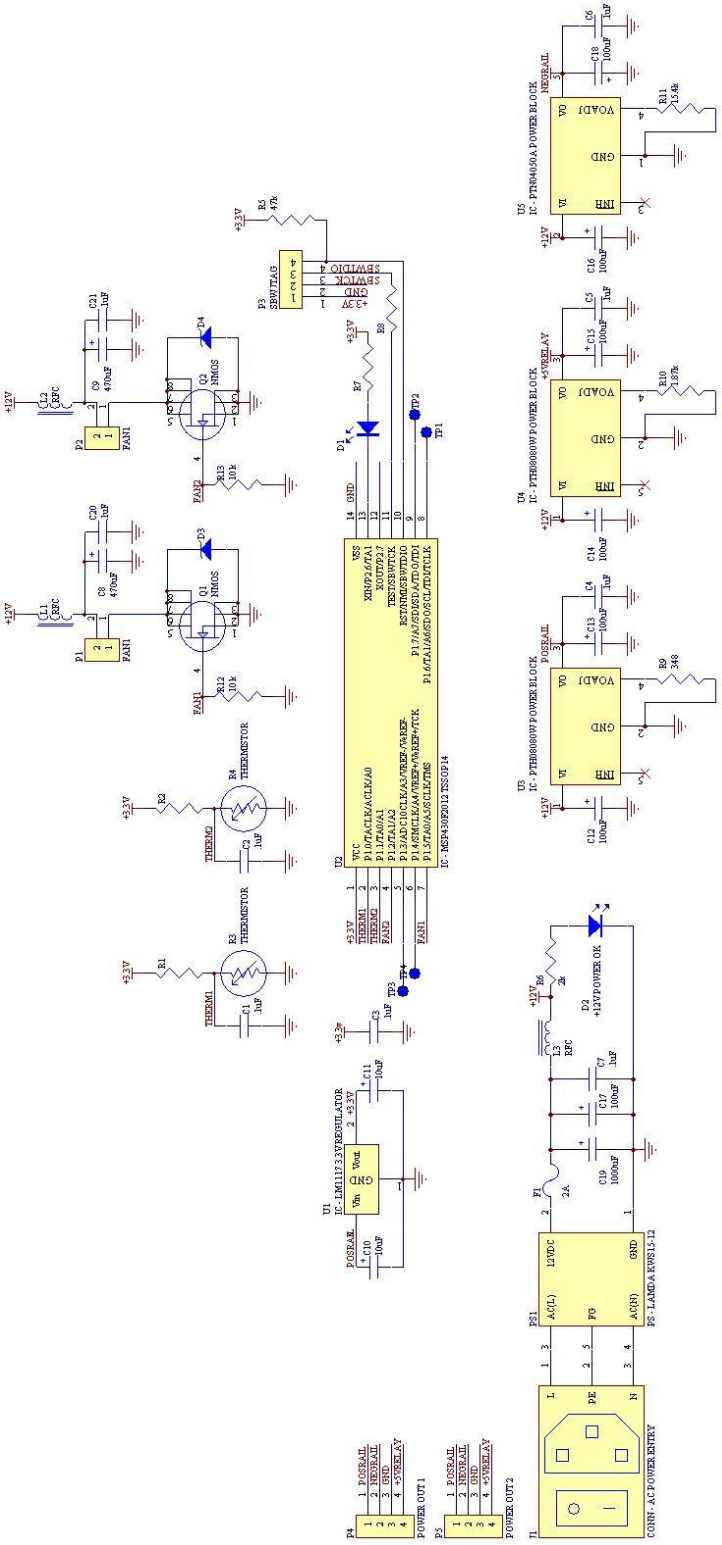


Figure 47: REV3 Power Supply Schematic

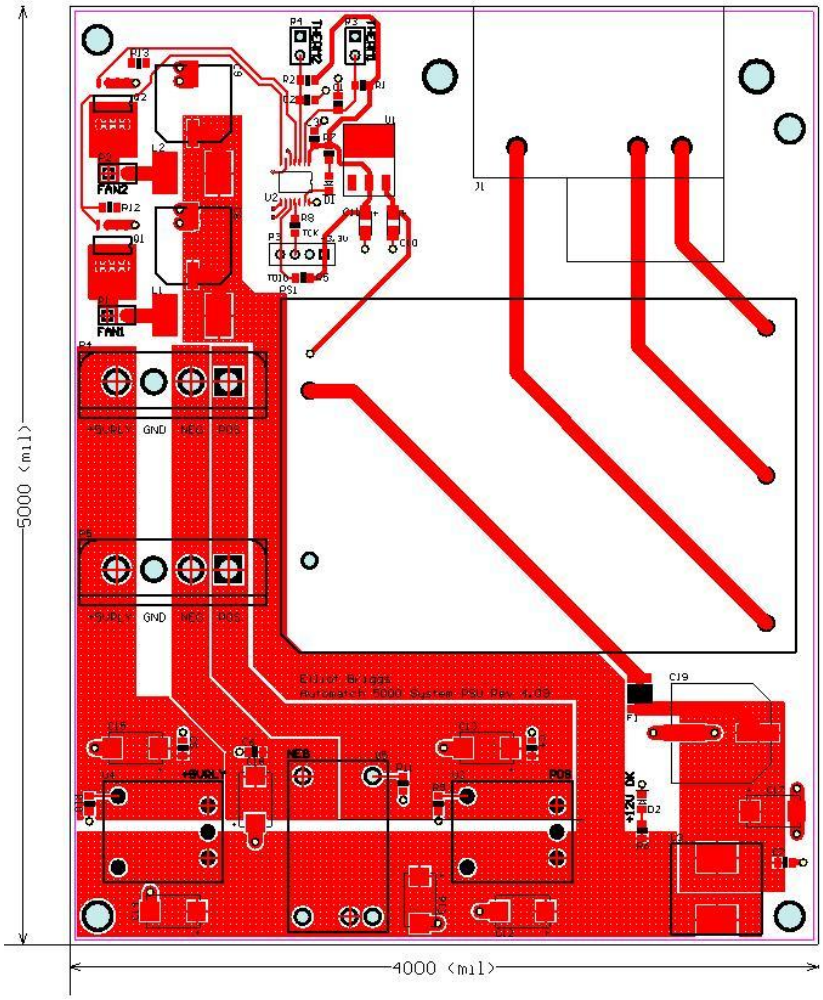


Figure 48: REV3 Power Supply PCB Layout Top

After three hardware revisions, a system has been created that is able to measure impedance and maximize power delivered to a load using feedback control. The hardware has been developed to be in a user friendly form factor and is able to provide measurement information through computer's serial port or on a text LCD screen for viewing.

Chapter 5

Testing and Results

The feedback control system that matches the load to appear as a real 50 Ω has been developed and tested. The control signal is derived directly from the phase and Zmag measurements as discussed in the 2.2 Measurement Methods section. In the following tests, the mechanisms implemented to handle the impedance matching process have been presented. In the case of an error condition, the control system is able to respond appropriately. The data displayed is recorded from the actual device through the Bluetooth modem on a PC terminal console.

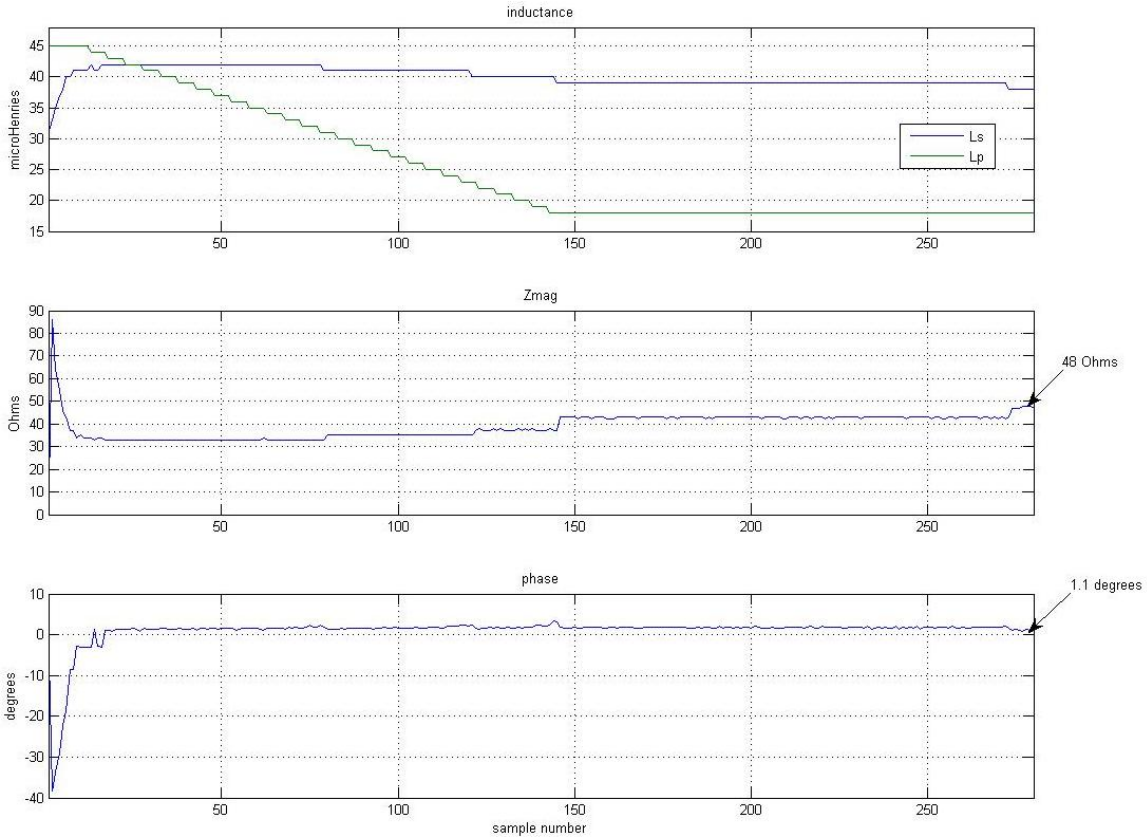


Figure 49: Automated Impedance Match Data Capture

Illustrated in Figure 49, a series 30 Ω resistor and 1.5 nF capacitor is matched to 50 Ω with a negligible phase angle (using a frequency of 800 kHz). When the acquisition procedure begins, the Lp and Ls inductors are switched to a default starting value of 32

μH and 45 μH respectively. These default values are somewhat arbitrary and have been chosen to provide a starting point for a relatively fast convergence. Immediately after the start of the matching process, the phase is quickly reduced to a small value, within about ±2 degrees. As the phase is adjusted to a near zero value, the Ls inductance increases to produce the necessary positive phase shift. After the phase has been corrected, the parallel inductor is adjusted, in this case reduced in value, to slowly increase the value of Zmag. As the parallel inductor is changed, the phase is also changed, which is quickly corrected by adjusting the series inductance Ls. The Ls control loop is designed so that phase can be corrected to a near zero value before the decision to change Lp must be made. The parallel inductor will adjust until Zmag is brought within a 10 Ω range of 50 Ω. In this case, the inductor stops adjusting when a Zmag of over 40 Ω is reached. The series inductor, however will continue to adjust until the phase is reduced to an acceptable level. Even when the parallel inductor is no longer adjusting, the series inductor will cancel out any phase outside of the range of acceptability.

Near the end of the plot, the phase is on the edge of the acceptable range and exceeds it for a brief moment, causing the series inductance to be reduced. After this inductance is reduced, the final Zmag value of 48 Ω is reached with a phase angle of 1.1 degrees. The inductor values that produce this result will be held indefinitely, providing the conditions remain constant. Any variations in load impedance will be responded to with proper inductor adjustment. If the control loop is not desired, possibly for chemistry tests where acoustic power conditions should not be varied suddenly by switching inductors, it can be disabled and re-enabled when desired. When disabled, the inductance values remain constant. Re-enabling the control system will cause the matching sequence to start from the default values.

It is possible that a load impedance can be out of the range of the device's capabilities. In this case, the control system must recognize when an error condition occurs. For example, if the control loop is requesting an inductance value that cannot be produced by the variable inductor, an error condition is present and must be handled. Such an error can occur when the control system's error signal cannot converge with the

variable inductors, and the inductance is driven out of range. Typically, when going through the matching process, the control loop will have found some matching conditions that do not fall into the window of acceptable ranges but produce a match that has an acceptable phase value and a non-ideal Zmag value. It is beneficial to store the matching condition with the best measured Zmag and phase in memory. In this process, the phase value is given priority; if the value of Zmag is acceptable but the phase value is not within 2 degrees of zero, the matching condition is not stored to memory. Having phase be nearly zero will likely produce more power transfer into the load than if the Zmag is acceptable but phase is not. By continuously checking and recording the best measured matching condition as the matching process occurs, the system can recall the inductance values used for the particular matching condition upon detecting an error. This control method yields a design that will always find the best possible matching condition that has been encountered, even if the ideal condition cannot be found.

Another matching sequence is illustrated in Figure 50. Here, the load is a series 15 Ω resistor and 1.5 nF capacitor. The frequency is set to 580 kHz. A lower frequency will produce a higher reactance given the same capacitance used in the previous test. The resistance of the previous test is halved for added impairment. The matching sequence appears to have a similar start as the previous example. The phase is quickly reduced and held to zero as the parallel inductor is adjusted. At a point, the parallel inductor is reduced to a very low value, making the reactance to ground very small. The value of Zmag is within the acceptable range, but the phase is intermittently passing through the boundary of this region, causing the series inductance to be slowly reduced. In this condition, large amounts of current will flow through the parallel inductor. Because a disproportionately large amount of current is flowing through the parallel inductor, the current through the load is reduced and the voltage at the point where the comparator is taking measurements is very low. When this occurs, errors in the phase measurement are encountered, and the series inductance is driven very abruptly to a very low value as large errors are accumulated over several samples. The inductance is driven to such a low level, that the control system eventually requests a negative inductance, triggering an error. Upon the

error condition, the negative inductance value is discarded and the recorded best matching condition is substituted. The system notifies the user that an error condition has been found, and the inductance values are no longer updated until user request. The system continues to measure phase and Zmag and displays the measurements on the LCD.

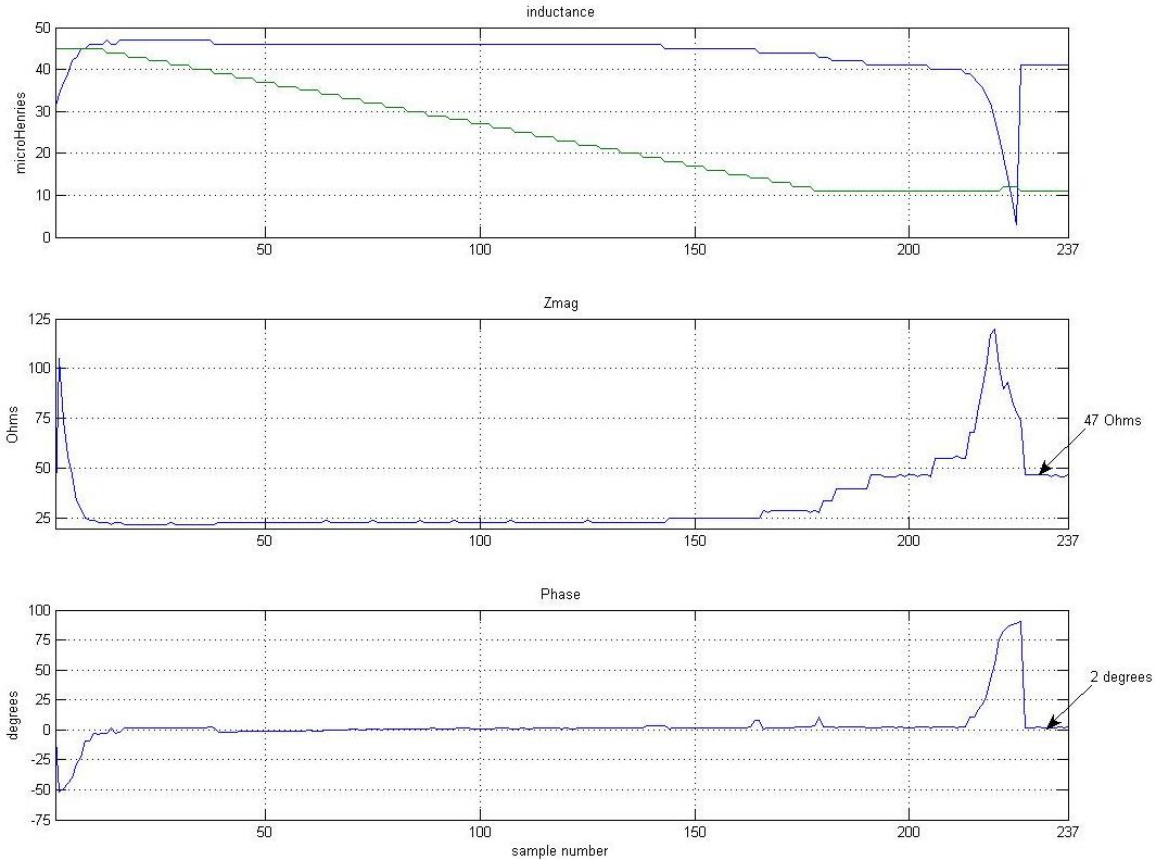


Figure 50: Error Condition Handled During Matching

In Figure 50, the best recorded matching condition is quite acceptable, but still out of the defined range. The reason the system continued correction instead of holding a constant value is due to the phase passing in and out of the acceptable range. For a brief period, the phase was found to be acceptable for the particular matching condition, and the inductance values were stored in memory. After some time, the phase drifted out of the acceptable range long enough to cause additional series inductance corrections. From this point, the phase measurement became invalid, and the error condition occurred. The

final impedance match result was 47 Ω and a phase of ~2 degrees after the best recorded match was applied.

The transducer, as described by Figure 33 and **Error! Reference source not found.**, exhibits a nonlinear relationship between the frequency and impedance. For some frequencies, the real resistance is very low, possibly as low as 9 Ω. A 9 Ω resistance with a nonzero reactance is difficult to transform to 50 Ω. Typically, matching a 9 Ω load with some reactance will produce an error. Such a load can be matched reliably up to the range of 20-35 Ω with a near-zero phase angle. If the resulting match is not the ideal 50 Ω with zero phase angle, the power delivered to the load is vastly greater than if no matching circuit was used. Hence, the impedance matching device is still providing valuable functionality.

A final test that measures the power increase introduced by the matching circuit is conducted. First, the impedance vs. frequency must be determined over the range of frequencies in the test. Figure 51 shows a narrow range of frequencies in which the transducer is designed to operate with Zmag, resistance, and capacitance measured by the system. By performing this frequency sweep, a baseline can be made to calculate the power ratio before and after the matching process has been carried out. Next, the system performed the matching process at each frequency, and the final result was recorded and presented in Figure 52. The phase for each result is within 3 degrees of zero and has been omitted in the diagram. Recall, the acceptable range of Zmag for the control system is between 40 Ω and 60 Ω.

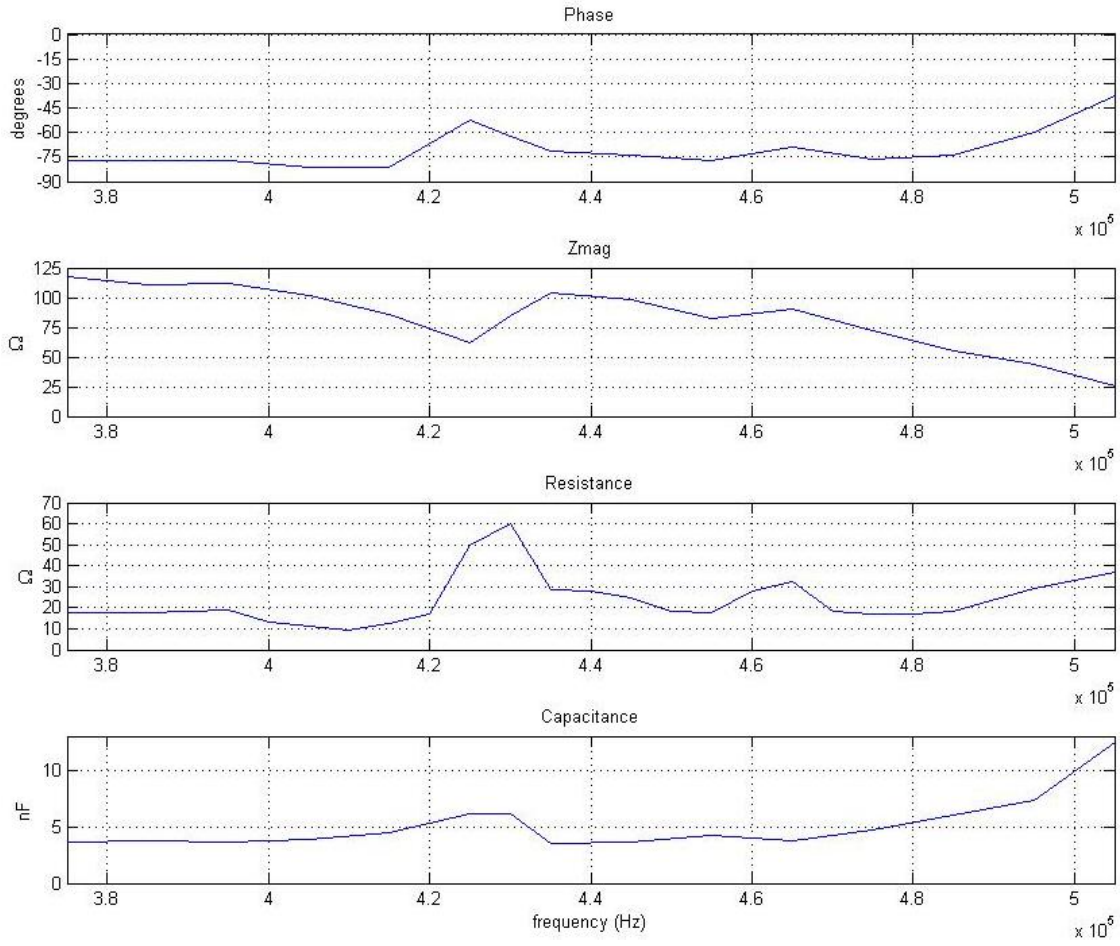


Figure 51: Transducer Impedance vs. Frequency

The test in Figure 52 was performed between 400 kHz and 480 kHz. This is the range of frequencies that were of interest to researchers performing experiments.

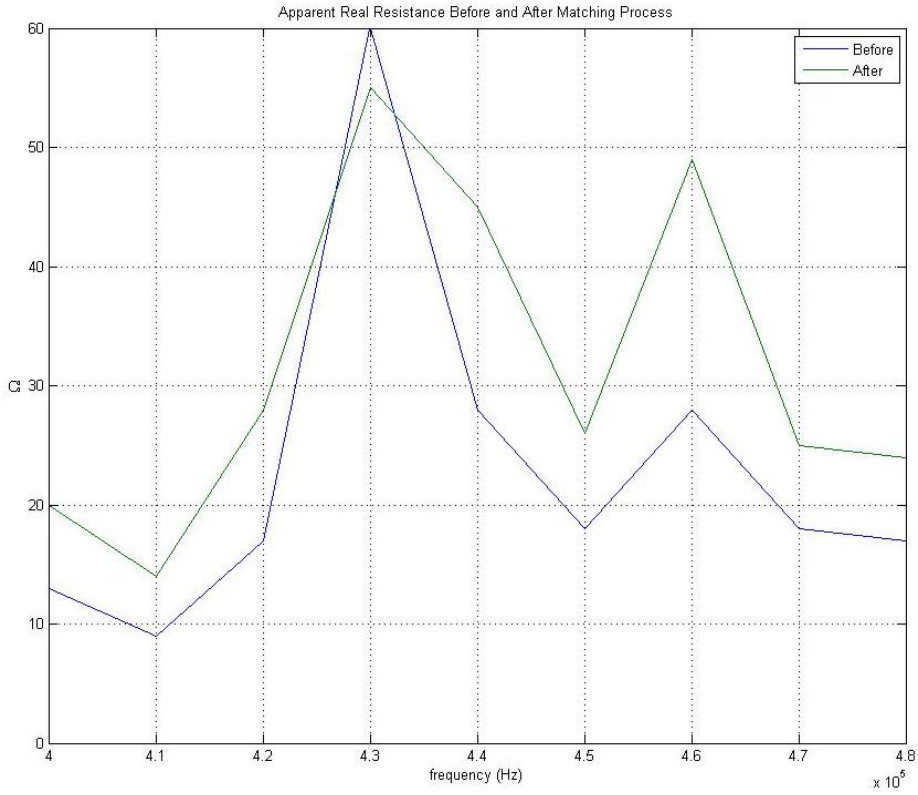


Figure 52: Resulting Zmag Before and After Matching Process

Using the formula for calculating the power delivered to a reactive load, the ratio of delivered power with the match relative to without was calculated and displayed in Figure 53. The power increase is dramatic when the capacitances are very small and reactance is high. In this case, large amounts of power increase are obtained by the cancellation of phase rather than increase in real resistance. At 430 kHz, the power is increased by the smallest amount, 130%. The real resistance at this frequency is measured to be 60 Ω, on the border of the window of acceptable values. The power is increased after the cancellation of phase and a slight reduction in real resistance. The power increase is slight because the impedance is already quite close to the target level without matching.

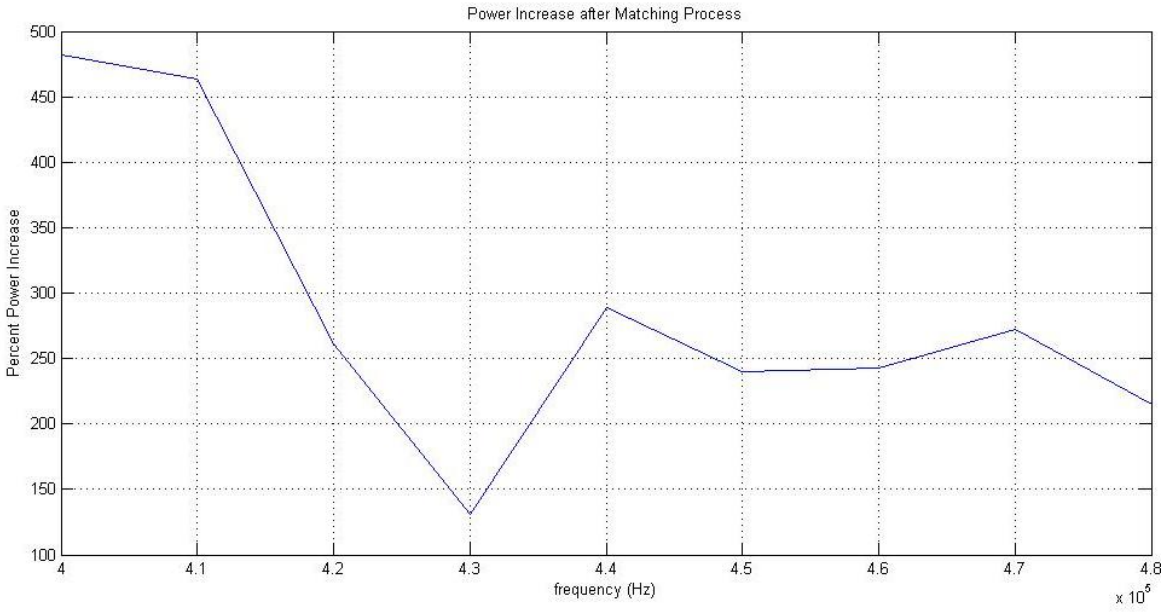


Figure 53: Power Increase after Matching Process

The above tests have displayed tests and information have displayed that the device is able to significantly increase power transfer into a reactive load. A power increase of up to 480% has been produced by the device. With such an increase in power, the device will be able to allow sonication at higher power levels or allow for a lower cost RF signal generator to be used.

Chapter 6

Conclusion

An automated impedance matching system has been created that will sense the impedance of an ultrasound transducer and match its impedance to the signal source's using a closed-loop feedback control system to deliver maximum power transfer. After extensive hardware development, verification and testing, a system is presented that can greatly increase the power delivered to a load with minimal human interaction required. The system that has been developed can operate over a wide range of ultrasonic frequencies, creating a product that is compatible with a wide variety of sonication applications. The system is also able to send measurement data and interact with a computer so that data-logging and digital control can be performed.

The chemistry research being performed requires the use of high power signals to produce heating and high pressure cavitations in a fluid. This application requires many watts of signal power. Future work includes testing and verification using a more powerful signal source that will be on the required level to perform the chemistry experiments. The control algorithm has been tested to a level that now allows higher power signals to be processed with a degree of safety.

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Appendix

The percent of maximum power transfer with a purely resistive load is shown as the load resistance is swept.

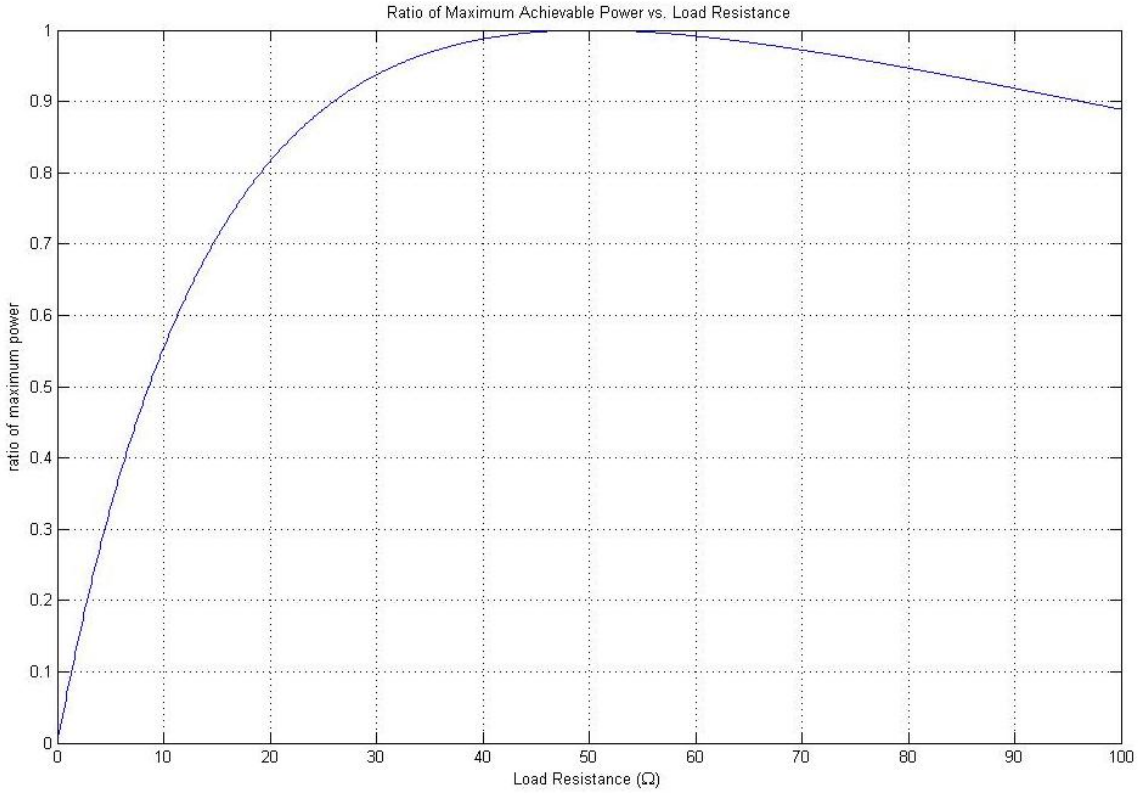

Figure 54: Load Resistance Sweep, Percent of Max Power Transfer